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Dossier technique
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EVALUATION KIT AVAILABLE

1.2GHz VCO with Linear Modulation Input

General Description

The MAX2754 self-contained, linear modulation, voltage-controlled oscillator (VCO) is intended for use in the 2.4GHz to 2.5GHz ISM band, particularly for FSK modulation systems that utilize a direct frequency-modulation transmit architecture. This device features a linear modulation input in addition to the standard frequency tuning input. The frequency tuning range of 1145MHz to 1250MHz (1/2 LO) also supports an IF up to 110MHz with low side LO. The VCO is based on Maxim's proprietary monolithic VCO technology, where all VCO components are integrated on-chip, including the varactor and inductor.

The MAX2754 linear modulation input offers a means to directly FM modulate the VCO with a constant modulation sensitivity over the tuning voltage input range. Typical frequency deviation is -500kHz/V which is linear to ±4% over the guaranteed frequency limits. The tuning input voltage range is +0.4V to +2.4V and the oscillator frequency is factory adjusted to provide guaranteed limits. The oscillator signal is buffered by an output amplifier stage (internally matched to 50Ω) to provide higher output power and isolate the oscillator from load impedance variations.

The MAX2754 operates over a +2.7V to +5.5V supply range. This device also provides a digitally controlled shutdown mode to permit implementation of sophisticated power-supply management. In shutdown, the supply current is reduced to 0.2µA. Even when active, power consumption is a modest 41mW.

The MAX2754 is packaged in the miniature 8-pin µMAX to offer the world's smallest, complete 2.4GHz direct-modulation VCO solution.

Applications

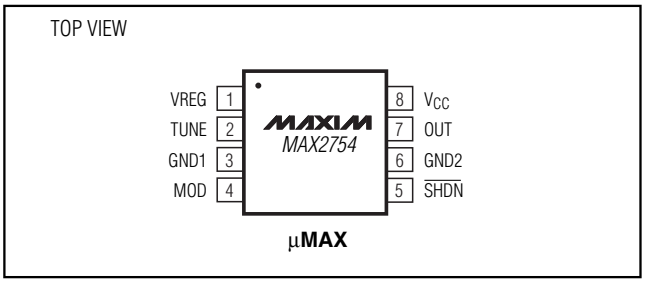
HomeRF WLAN

Bluetooth

2.4GHz Cordless Phones

2.4GHz Wireless Data Radios

Pin Configuration



Features

- ♦ **Fully Monolithic VCO Construction with On-Chip Inductor and Varactor Tuning Elements**
- ♦ **Guaranteed 1145MHz to 1250MHz Tuning Range to Support 1/2 LO Applications**
- ♦ **Modulation Linearity Within ±4%**
- ♦ **Precise Modulation Gain (-500kHz/V)**
- ♦ **Low Phase Noise (-137dBc/Hz at 4MHz offset)**
- ♦ **+2.7V to +5.5V Single-Supply Operation**
- ♦ **Low-Current Shutdown Mode**
- ♦ **Miniature 8-Pin µMAX® Package**

Ordering Information

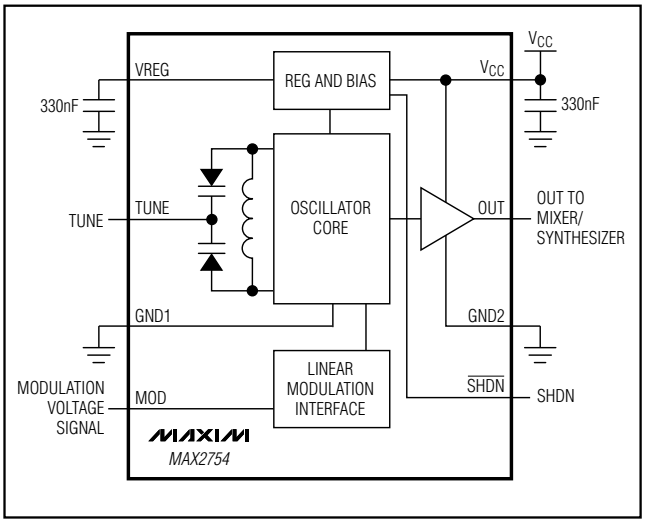
PART	TEMP RANGE	PIN-PACKAGE
MAX2754EUA	-40°C to +85°C	8 µMAX

8-pin µMAX

(3mm × 5mm)

µMAX is a registered trademark of Maxim Integrated Circuits, Inc.

Typical Operating Circuit



1.2GHz VCO with Linear Modulation Input

ABSOLUTE MAXIMUM RATINGS

V_{CC} to GND .....-0.3V to +6.0V
VREG to GND .....-0.3V to +6.0V
TUNE, $\overline{SHDN}$, MOD to GND .....-0.3V to (V_{CC} + 0.3V)
OUT to GND .....-0.3V to +6.0V
Continuous Power Dissipation (T_A = +70°C)
8-Pin µMAX (derate 5.7mW/°C above T_A = +70°C) 457mW

Operating Temperature Range .....-40°C to +85°C
Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +160°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION! ESD SENSITIVE DEVICE

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.7V to +5.5V, V_{TUNE} = +0.4V to +2.4V, $V_{\overline{SHDN}} \geq$ +2.0V, V_{MOD} = +1.4V, OUT is connected to a 50Ω load, T_A = -40°C to +85°C. Typical values are at V_{CC} = +3.0V, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}		2.7		5.5	V
Supply Current	I_{CC}	T_A = +25°C, $V_{\overline{SHDN}} \geq$ 2.0V		13.7	19	mA
		T_A = -40°C to +85°C, $V_{\overline{SHDN}} \geq$ 2.0V			20	
		$V_{\overline{SHDN}} \leq$ 0.6V	-2	0.2	2	µA
Digital Input Voltage High	V_{IH}		2.0			V
Digital Input Voltage Low	V_{IL}				0.6	V
Digital Input Current High	I_{IH}	$V_{\overline{SHDN}} \geq$ 2.0V	-2		2	µA
Digital Input Current Low	I_{IL}	$V_{\overline{SHDN}} \leq$ 0.6V	-1		1	µA
Modulation Input Voltage Range	V_{MOD}		0.4		2.4	V
TUNE Leakage Current (Note 2)		V_{TUNE} = +0.4V to +2.4V		0.01		nA

AC ELECTRICAL CHARACTERISTICS

(MAX2754 EV kit. V_{CC} = +2.7V to +5.5V, V_{TUNE} = +0.4V to +2.4V, $V_{\overline{SHDN}} \geq$ +2.0V, V_{MOD} = +1.4V, OUT is connected to a 50Ω load, T_A = +25°C. Typical values are at V_{CC} = +3.0V, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Oscillator Guaranteed Frequency Limits	f_{MIN}, f_{MAX}	V_{TUNE} = +0.4V to +2.4V, T_A = -40°C to +85°C	1145		1250	MHz
Phase Noise		f_{OFFSET} = 4MHz		-137		dBc/Hz
		Noise floor		-151		dBm/Hz
Tuning Gain		V_{TUNE} at f_{MIN}		124		MHz/V
		V_{TUNE} at f_{MAX}		81		
Output Power				-5		dBm
Modulation Peak Frequency Deviation		$f_{MIN} < f < f_{MAX}$ (Note 2)	±400	±500	±600	kHz
Modulation Sensitivity		Common-mode V_{MOD} = 1.4V		-500		kHz/V

AC ELECTRICAL CHARACTERISTICS (continued)

(MAX2754 EV kit. V_{CC} = +2.7V to +5.5V, V_{TUNE} = +0.4V to +2.4V, $V_{\overline{SHDN}} \geq$ +2.0V, V_{MOD} = +1.4V, OUT is connected to a 50Ω load, T_A = +25°C. Typical values are at V_{CC} = +3.0V, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Modulation Linearity		V_{MOD} = +0.4 to +2.4V, $f_{MIN} < f < f_{MAX}$ (Note 4)		±4		%
Modulation Full-Power Bandwidth (Note 5)				2.5		MHz
Return Loss (Note 6)		$f_{MIN} < f < f_{MAX}$		7.5		dB
Output Harmonics				-20		dBc
Load Pulling		VSWR = 2:1, all phases		1.5		MHz_{p-p}
Supply Pushing		V_{CC} stepped: +3.3V to +2.8V		0.16		MHz/V
Oscillator Turn-On Time (Note 7)				10		µs
Oscillator Turn-Off Time (Note 8)				8		µs

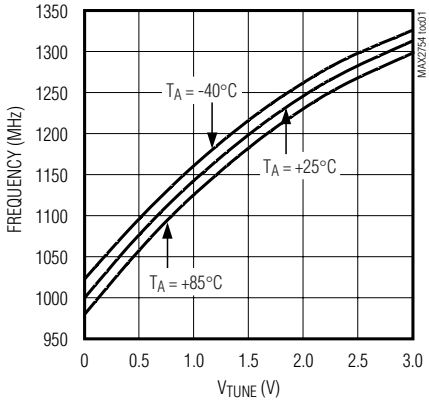
Note 1: Specifications are production tested at T_A = +25°C. Limits over temperature are guaranteed by design and characterization.
Note 2: Limits are guaranteed by production test at +25°C.
Note 3: Center point is nominally +1.4V.
Note 4: Maximum variation in the modulation sensitivity from its average value over the guaranteed frequency limits.
Note 5: Bandwidth is defined as the point where the response to the modulation port is 0.707 times the low-frequency response. Bandwidth limits on the modulation input for a 1Vp-p sine wave. Common-mode V_{MOD} = +1.4V.
Note 6: Refer to *Output Buffer* section for suggestions to improve the return loss to 12dB.
Note 7: Turn-on time to within 3dB of final output power.
Note 8: Turn-off time to output power of -10dBm.

1.2GHz VCO with Linear Modulation Input

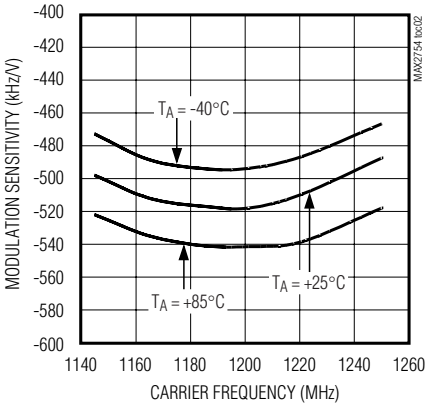
Typical Operating Characteristics

(MAX2754 EV kit, V_{CC} = +3.0V, $V_{\overline{SHDN}} \geq$ +2.0V, $V_{TUNE} = V_{MOD}$ = +1.4V, and T_A = +25°C, unless otherwise noted.)

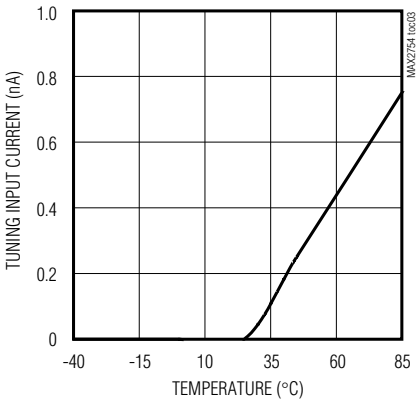
VCO TUNING CURVE



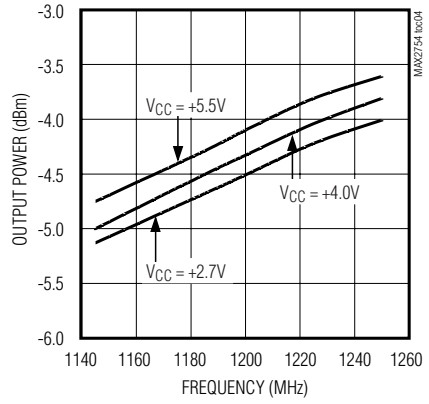
MODULATION SENSITIVITY vs. CARRIER FREQUENCY



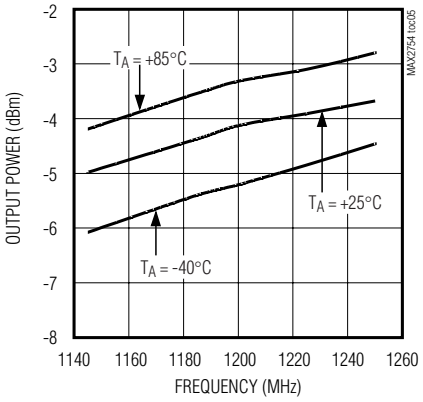
TUNE INPUT CURRENT vs. TEMPERATURE



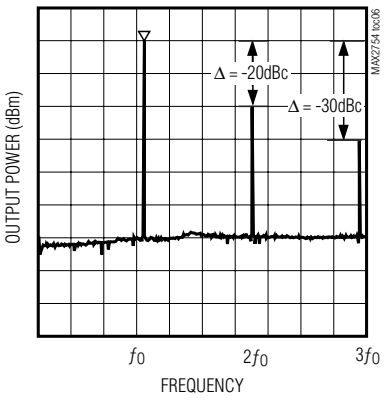
OUTPUT POWER vs. FREQUENCY



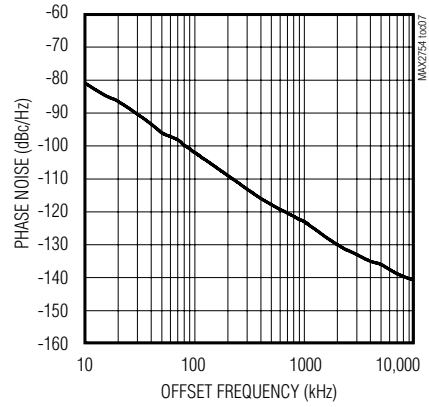
OUTPUT POWER vs. FREQUENCY



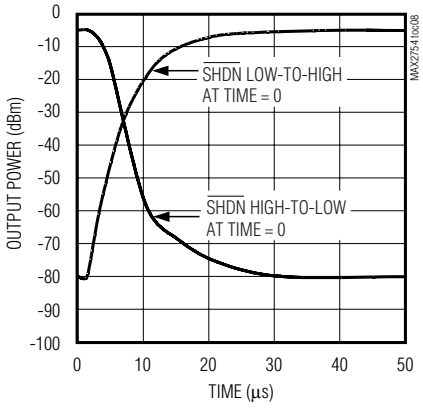
NORMALIZED HARMONIC OUTPUT SPECTRUM



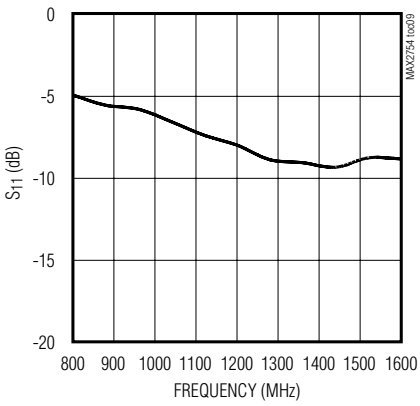
PHASE NOISE



OSCILLATOR TURN-ON/ TURN-OFF TIME



OUTPUT S_{11}



Pin Description

PIN	NAME	FUNCTION
1	VREG	Capacitor Connection to the On-Chip Linear Regulator Output. Connect a 330nF capacitor to ground.
2	TUNE	Oscillator Frequency Tuning-Voltage Input. High-impedance input with a voltage range of +0.4V (low frequency) to +2.4V (high frequency).
3	GND1	Ground Connection for the Oscillator Core. Requires a low-inductance connection to the circuit-board ground plane.
4	MOD	Linear Modulation Input. High-impedance CMOS input with a voltage range of +0.4V to +2.4V.
5	$\overline{SHDN}$	Shutdown Input. Drive logic low to place the device in shutdown mode. Drive logic high for normal operation.
6	GND2	Ground Connection for Output-Buffered Amplifier, Linear Modulation Interface, and Biasing. Requires a low-inductance connection to the circuit-board ground plane.
7	OUT	Buffered Oscillator Output. Incorporates an internal DC-blocking capacitor. OUT is internally matched to 50Ω.
8	V_{CC}	Supply Voltage Connection. Requires external RF bypass capacitor to ground for low noise and low spurious content performance from the oscillator. Bypass with a 330pF capacitor to ground.

Detailed Description

Oscillator

The MAX2754 VCO is implemented as an LC oscillator topology, integrating all of the tank components on-chip. This fully monolithic approach provides an extremely easy-to-use VCO, equivalent to a VCO module. The frequency is controlled by a voltage applied to the TUNE pin. The VCO core uses a differential topology to provide a stable frequency versus supply voltage and improve the immunity to load variations. In addition, there is a buffer amplifier following the oscillator core to provide added isolation from load and supply variations and to boost the output power.

Linear Modulation

The linear modulation input offers a means to directly FM modulate the VCO with a controlled amount of frequency deviation for a given input voltage deviation. The unique technique maintains a consistent modulation gain (df/dV_{MOD}) across the entire frequency tuning range of the part, enabling accurate FM modulation derived solely from the filtered NRZ “data” stream (the modulation voltage input).

The modulation input is single-ended and centered about +1.4V. The linear modulation full-scale range is ±1V around this point, for a +0.4V to +2.4V input voltage range. A very important point to note is that the sign of the modulation gain is negative. A positive change in V_{MOD} results in a negative change in oscillation frequency. This convention for the modulation gain is due to the practical implementation of the internal linearizing circuitry. This gain inversion must be considered when designing the analog voltage interface that drives the linear modulation input. The easiest way to handle this is to invert the logic polarity of the modulation data three-state output buffer (TX data output). Where it is impossible to invert the data-stream logic polarity, an external inverter and three-state buffer would be required. These devices are offered in small single-logic gates in SC-79 style packages from various manufacturers (e.g., Fairchild—Tiny Logic, On Semiconductor, or Rohm).

Figure 1 illustrates the frequency versus V_{MOD} characteristic of the modulation input. Note the negative slope of the curve, $df_{MOD}/dV_{MOD} < 0$, where $f_{MOD} = f_{OUT} - f_{NOM}$.

Output Buffer

The oscillator signal from the core drives an output buffer amplifier. The amplifier is internally matched to 50Ω including an on-chip DC-blocking capacitor. The return loss can be improved to a minimum of 12dB over 1145MHz to 1250MHz by adding a 2.5nH series inductor and a 3.0pF shunt capacitor. The output buffer has a ground connection separate from the oscillator core to minimize load-pulling effects. The amplifier boosts the oscillator signal to a level suitable for driving most RF mixers.

1.2GHz VCO with Linear Modulation Input

Applications Information

Tune Input

The tuning input is typically connected to the output of the PLL loop filter. The loop filter provides an appropriately low-impedance source. Incorporate an extra RC filter stage to reduce high-frequency noise and spurious signals. Any excess noise on the tuning input is directly translated into FM noise, which can degrade the phase-noise performance of the oscillator. Therefore, it is important to minimize the noise introduced on the tuning input. A simple RC filter with low corner frequency is needed during testing to filter the noise present on the voltage source driving the tuning line.

Two-Level FSK Applications

The MAX2754 is designed for use in FSK applications operating in the 2.4GHz to 2.5GHz ISM band. Specifically, it is targeted for those systems which utilize a direct TX modulation architecture in which the VCO is directly modulated with the data signal during the transmit (TX) mode. The VCO in these systems runs at half the RF output frequency and is used in conjunction with a frequency doubler to produce the final LO signal for both RX and TX modes of operation.

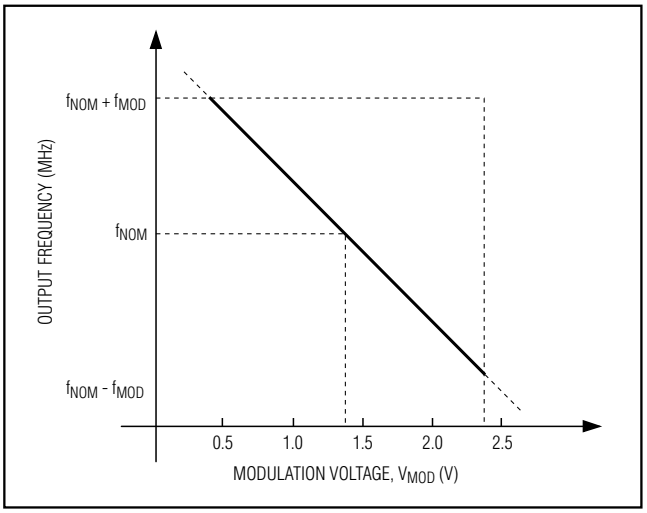


Figure 1. Modulation Frequency Deviations Characteristics

Figure 2 shows a typical applications circuit. To compute R1, R2, R3, and R4, determine the modulation voltage center point (V_{MODB} = +1.4V). Compute the required modulation voltage deviation as follows:

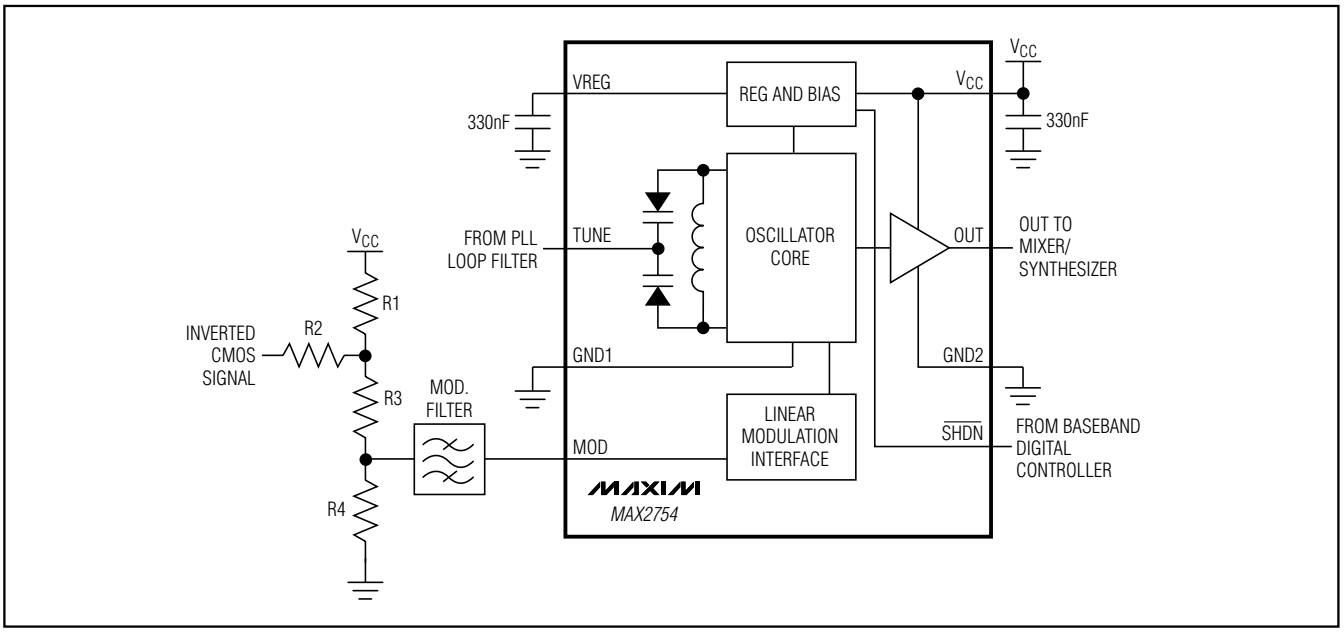


Figure 2. Typical Application Circuit for Two-Level FSK

$\Delta V = \Delta f$ / 500kHz/V (nominal modulation sensitivity)

Let $R = R_1 + R_3 + R_4$. Setting R based on the desired current from V_{CC} and filter impedance level:

$$R1 = \frac{R}{2},$$

$$R2 = \left(\frac{V_{MODB}}{\Delta V} - 1 \right) \times \frac{R}{4},$$

$$R3 = R \times \left(\frac{1}{2} - \frac{V_{MODB}}{V_{CC}} \right),$$

$$R4 = \frac{V_{MODB}}{V_{CC}} \times R$$

Layout Issues

Use controlled impedance lines (microstrip, co-planar waveguide, etc.) each time for high-frequency signals. Always place decoupling capacitors as close to the V_{CC} pins as possible; for long V_{CC} lines, it may be necessary to add additional decoupling capacitors located further from the device. Always provide a low-inductance path to ground, and keep GND vias as close to the device as possible. Thermal reliefs on GND pads are not recommended.

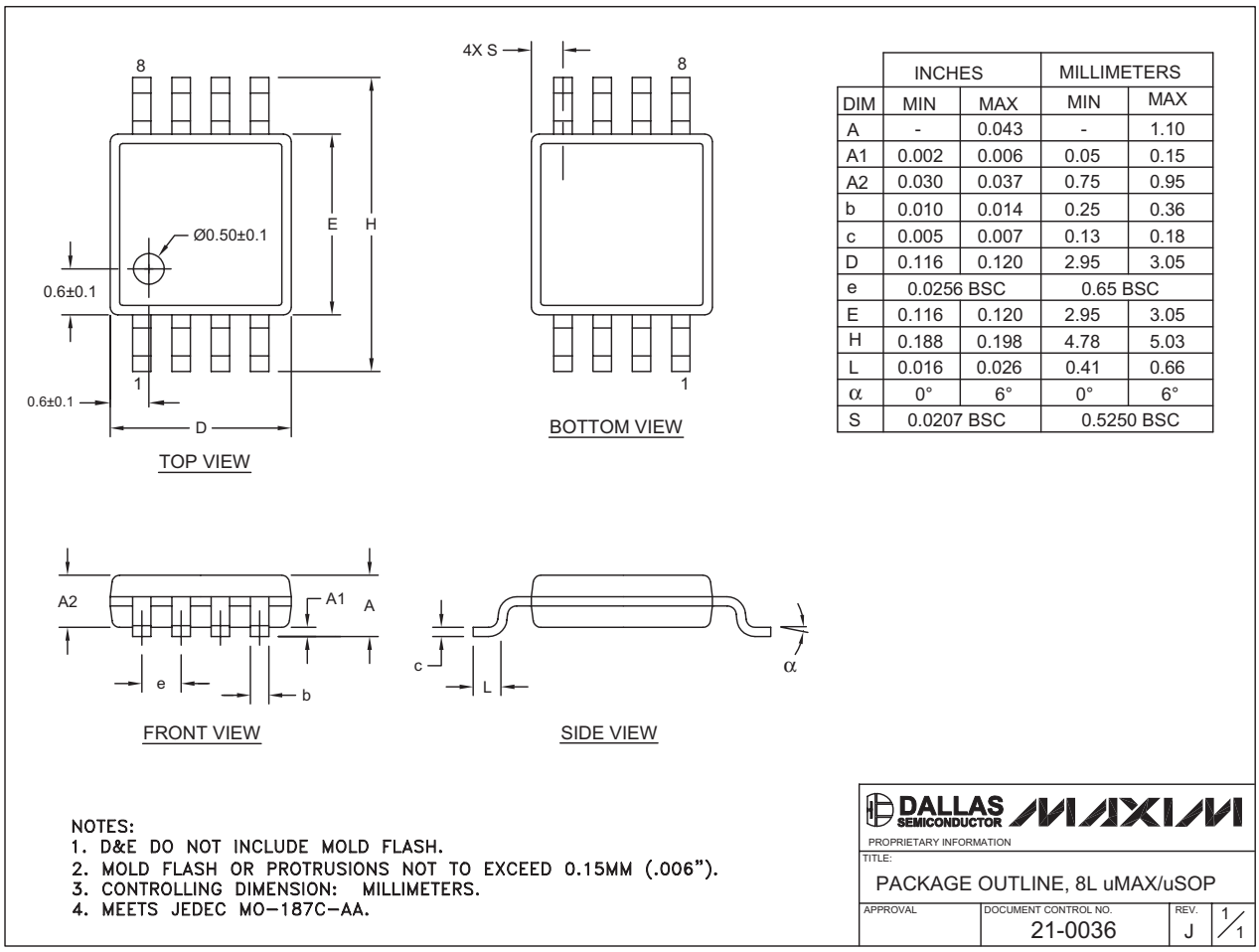
Chip Information

TRANSISTOR COUNT: 619

1.2GHz VCO with Linear Modulation Input

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	-	0.043	-	1.10
A1	0.002	0.006	0.05	0.15
A2	0.030	0.037	0.75	0.95
b	0.010	0.014	0.25	0.36
c	0.005	0.007	0.13	0.18
D	0.116	0.120	2.95	3.05
e	0.0256 BSC		0.65 BSC	
E	0.116	0.120	2.95	3.05
H	0.188	0.198	4.78	5.03
L	0.016	0.026	0.41	0.66
α	0°	6°	0°	6°
S	0.0207 BSC		0.5250 BSC	

MONOLITHIC AMPLIFIERS 50Ω

BROADBAND DC to 8 GHz


ERA


ERA-SM

low power, up to +13.5 dBm output

all specifications at 25°C

MODEL◆ NO.	✪ FREQ. GHz f_L - f_u	GAIN, dB Typical over frequency, GHz 0.1	1	2	3	4	6	8	Min.@ 2 GHz	Flatness DC- 2 GHz	MAXIMUM POWER (dBm) at 2 GHz* Output (1 dB Comp.) Typ.	Min.	Input (no dmg)	DYNAMIC RANGE at 2 GHz* NF (dB) Typ.	IP3 (dBm) Typ.	VSWR (:1) Typ. In DC-3 GHz	3-f_u** GHz	Out DC-3 GHz	3-f_u** GHz	ABSO-LUTE MAX. RATING[3] I (mA)	P (mW)	DC OPERATING POWER[4] at Pin 3 Current (mA)	Volt. Typ	Min	Max	THERMAL RESIS-TANCE θjc Typ. °C/W	CASE STYLE Note B	CONNECTION	PRICE $ Qty. (30)
ERA-1	DC-8	12.3	12.1	11.8	10.9	9.7	7.9	8.2	9	±0.3	12.0	10.0	15	4.3	26	1.5	1.8	1.5	1.9	75	330	40	3.4	3.0	4.1	178	VV105	cb	1.37
ERA-2	DC-6	16.2	15.8	15.2	14.4	13.1	11.2	—	13	±0.5	13.0	11.0	15	4.0	26	1.3	1.4	1.2	1.6	75	330	40	3.4	3.0	4.1	155	VV105	cb	1.52
ERA-3	DC-3	22.1	21.0	18.7	16.8	—	—	—	16	±1.7	12.5	9	13	3.5	25	1.5	—	1.4	—	75	330	35	3.2	3.0	4.1	154	VV105	cb	1.67
ERA-1SM	DC-8	12.3	12.1	11.8	10.9	9.7	7.9	8.2	9	±0.3	12.0	10.0	15	4.3	26	1.5	1.8	1.5	1.9	75	330	40	3.4	3.0	4.1	183	WW107	cb	1.42
NEW ERA-21SM	DC-8	14.2	13.9	13.2	12.2	10.8	8.7	8.9	11.2	±0.5	12.6	10.6	15	4.7	26	1.1	1.4	1.3	1.9	75	330	40	3.5	3.0	4.1	194	WW107	cb	1.57
ERA-2SM	DC-6	16.2	15.8	15.2	14.4	13.1	11.2	—	13	±0.5	13.0	11.0	15	4.0	26	1.3	1.4	1.2	1.6	75	330	40	3.4	3.0	4.1	160	WW107	cb	1.57
NEW ERA-33SM	DC-3	19.3	18.7	17.4	15.9	—	—	—	15	±0.9	13.5	11.5	13	3.9	28.5	1.6	—	1.25	—	75	330	40	4.3	3.8	4.8	140	WW107	cb	1.72
ERA-3SM	DC-3	22.1	21.0	18.7	16.8	—	—	—	16	±1.7	12.5	9	13	3.5	25	1.5	—	1.4	—	75	330	35	3.2	3.0	4.1	159	WW107	cb	1.72

features

- low thermal resistance
- miniature microwave amplifier
- available in drop-in & surface mount (sm) versions
- frequency range, DC to 8 GHz, usable to 10 GHz
- up to 18.5 dBm typ. (16.5 dBm min) output power

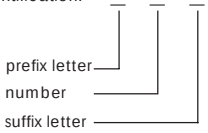
absolute maximum ratings

operating temperature: -45°C to 85°C
storage temperature: -65° to 150°C

model identification

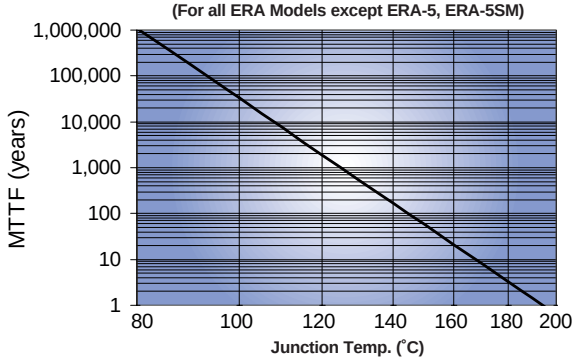
Model	marking (see note below)
ERA-1, ERA-1SM	1
ERA-2, ERA-2SM	2
ERA-21SM	21
ERA-3, ERA-3SM	3
ERA-33SM	33
ERA-4, ERA-4SM	4
ERA-5, ERA-5SM	5
ERA-50SM	50
ERA-51SM	51
ERA-6, ERA-6SM	6

Note: Prefix letter (optional) designates assembly location. Suffix letters (optional) are for wafer identification.



NOTES:

◆ Aqueous washable
* at 1 GHz for ERA-4,5,6, 4SM, 5SM, 50SM, 51SM, 6SM
** f_u is the upper frequency limit for each model as shown in the table.
*** Gain, gain flatness, and VSWR are specified at 1.5 GHz.
✪ Low frequency cutoff determined by external coupling capacitors.
A. Environmental specifications and re-flow soldering information available in General Information Section.
B. Units are non-hermetic unless otherwise noted. For details on case dimensions & finishes see "Case Styles & Outline Drawings".
C. Prices and Specifications subject to change without notice.
D. For Quality Control Procedures see Table of Contents, Section 0, "Mini-Circuits Guarantees Quality" article. For Environmental Specifications see Amplifier Selection Guide.
1. Model number designated by alphanumeric code marking.
2. ERA-SM models available on tape and reel.
3. Permanent damage may occur if any of these limits are exceeded. These ratings are not intended for continuous normal operation.
4. Supply voltage must be connected to pin 3 through a bias resistor in order to prevent damage. See "Biasing MMIC Amplifiers" in minicircuits.com/application.html. Reliability predictions are applicable at specified current & normal operating conditions.



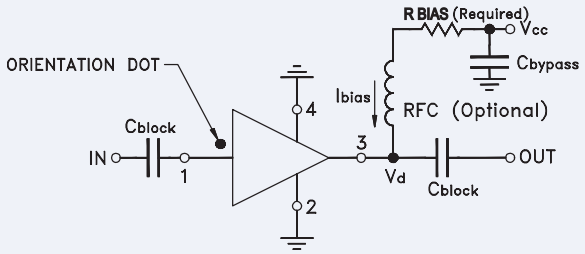
011217

medium power, up to +18.4 dBm output

all specifications at 25°C

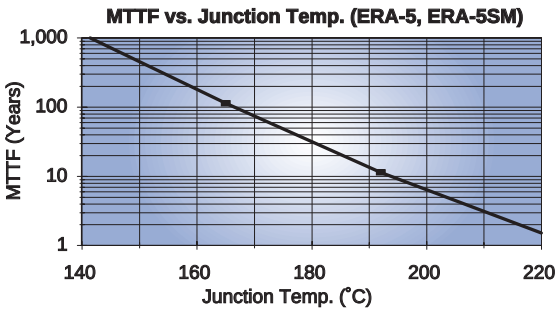
MODEL◆ NO.	✪ FREQ. GHz f_L - f_u	GAIN, dB Typical over frequency, GHz 0.1	1	2	3	4	6	8	Min.@ 2 GHz	Flatness DC- 2 GHz	MAXIMUM POWER (dBm) at 2 GHz* Output (1 dB Comp.) Typ.	Min.	Input (no dmg)	DYNAMIC RANGE at 2 GHz* NF (dB) Typ.	IP3 (dBm) Typ.	VSWR (:1) Typ. In DC-3 GHz	3-f_u** GHz	Out DC-3 GHz	3-f_u** GHz	ABSO-LUTE MAX. RATING[3] I (mA)	P (mW)	DC OPERATING POWER[4] at Pin 3 Current (mA)	Volt. Typ	Min	Max	THERMAL RESIS-TANCE θjc Typ. °C/W	CASE STYLE Note B	CONNECTION	PRICE $ Qty. (30)
ERA-6	DC-4	12.6	12.5	12.2	11.7	11.3	—	—	10.5	±0.2	17.9	16	20	4.5	36	1.3	1.2	1.6	1.8	120	650	70	5.0	4.6	5.6	170	VV105	cb	3.85
ERA-4	DC-4	14.3	14.0	13.4	12.7	11.8	—	—	11	±0.4	17.3	15	20	4.2	34	1.2	1.2	1.3	1.8	120	650	65	4.5	4.2	5.5	163	VV105	cb	3.85
ERA-5	DC-4	20.2	19.5	18.5	17.3	16.2	—	—	16	±1.0	18.4	16.5	13	4.3	32.5	1.3	1.3	1.2	1.3	120	650	65	4.9	4.2	5.5	278	VV105	cb	3.85
ERA-6SM	DC-4	12.6	12.5	12.2	11.7	11.3	—	—	10.5	±0.2	17.9	16	20	4.5	36	1.3	1.2	1.6	1.8	120	650	70	5.0	4.6	5.6	175	WW107	cb	3.90
ERA-4SM	DC-4	14.3	14.0	13.4	12.7	11.8	—	—	11	±0.4	17.3	15	20	4.2	34	1.2	1.2	1.3	1.8	120	650	65	4.5	4.2	5.5	168	WW107	cb	3.90
NEW ERA-51SM	DC-4	18.0	17.4	16.1	14.8	12.5	—	—	14	±1.0	18.1	16.5	13	4.1	33	1.1	1.2	1.2	1.9	120	650	65	4.5	4.2	5.5	154	WW107	cb	3.90
ERA-5SM	DC-4	20.2	19.5	18.5	17.3	16.2	—	—	16	±1.0	18.4	16.5	13	4.3	32.5	1.3	1.3	1.2	1.3	120	650	65	4.9	4.2	5.5	283	WW107	cb	3.90
NEW ERA-50SM***	DC-1.5	20.7	19.4	18.3	—	—	—	—	16	±1.2	17.2	16.0	13	3.5	32.5	1.3	—	1.2	—	120	650	60	4.4	4.0	4.9	177	WW107	cb	2.95

typical biasing configuration



R BIAS
"1%" Resistor Values (ohms) for Optimum Biasing of ERA Models

Vcc	ERA-1, 1SM	ERA-2, 2SM	ERA-21SM	ERA-3, 3SM	ERA-33SM	ERA-4, 4SM	ERA-5, 5SM	ERA-50SM, 51SM	ERA-6, 6SM
7	90.9	88.7	88.7	107	69.8	38.3	40.2	40.2	30.1
8	113	113	113	133	93.1	52.3	53.6	53.6	43.2
9	137	137	137	162	115	66.5	68.1	68.1	56.2
10	162	162	162	191	140	80.6	82.5	82.5	69.8
11	187	187	187	221	165	95.3	97.6	97.6	84.5
12	215	215	210	249	191	110	113	113	97.6
13	237	237	237	280	215	127	127	127	113
14	261	261	261	309	243	143	143	143	127
15	287	287	287	340	267	158	158	158	140
16	309	316	316	365	287	174	174	174	154
17	332	340	340	392	316	187	191	191	169
18	357	365	365	422	340	205	205	205	182
19	383	392	392	453	365	221	221	221	196
20	412	412	412	475	392	237	237	237	210



designers kits available

KIT NO.	Model Type	No. of Units in Kit	Description	Price $ per kit
K1-ERA	ERA	30	10 of each 1,2,3	49.95
K2-ERA	ERA	20	10 of each 4,5	69.95
K1-ERASM	ERA-SM	30	10 of each 1SM, 2SM,3SM	49.95
K2-ERASM	ERA-SM	20	10 of each 4SM, 5SM	69.95
K3-ERASM	ERA-SM	30	10 of each 4SM, 5SM, 6SM	99.95

pin connections

PORT	cb
RF IN	1
RF OUT	3
DC	3
CASE GND	2,4
NOT USED	—

NSN GUIDE

MCL NO.	NSN
ERA-1SM	5962-01-459-9075
ERA-2SM	5962-01-459-7410
ERA-3SM	5962-01-459-9314

010621

High Directivity

Monolithic Amplifier 0.5-2.5 GHz

Product Features

- 3V & 5V operation
- no external biasing circuit required
- internal DC blocking at RF input and output
- high directivity, 20 dB typ.
- wide bandwidth, 0.5 to 2.5 GHz
- low noise figure, 5.5 dB typ.
- output power, up to +18.2 dBm typ.
- low cost

VNA-25+

CASE STYLE: XX211-1
PRICE: $2.50 ea. QTY. (25)

+ RoHS compliant in accordance with EU Directive (2002/95/EC)

The +Suffix has been added in order to identify RoHS Compliance. See our web site for RoHS Compliance methodologies and qualifications.

Typical Applications

- buffer amplifier
- cellular
- PCN

General Description

VNA-25+ is a wideband amplifier offering high dynamic range. It has repeatable performance from lot to lot. It is enclosed in an 8-lead SOIC package. VNA-25+ is fabricated using GaAs MESFET technology. Expected MTBF at 85°C case temperature is 40,000 years at 2.8V, 2,000 at 5V.

Pin Description

Function	Pin Number	Description
RF IN	3	RF input pin.
RF OUT	6	RF output pin.
DC	1	Bias pin
GND	2,4,5,7,8	Connections to ground. Use via holes as shown in “Suggested Layout for PCB Design” to reduce ground path inductance for best performance.

Electrical Specifications at 25°C

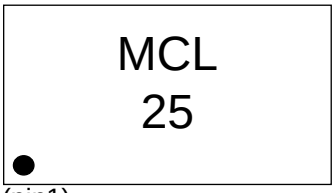
Parameter		Min.	Typ.		Max.	Units
Frequency Range		0.5			2.5	GHz
at DC Volts		5.0	5.0	2.8	5.0	V
Gain	f=0.5 GHz f=1.0 GHz f=1.5 GHz f=2.0 GHz f=2.5 GHz	16	15.5 18.0 18.6 17.8 16	14.5 16.7 17.4 17 15.5		dB
Input Return Loss	f=0.75 to 2.5 GHz		14	14		dB
Output Return Loss	f=0.75 to 2.5 GHz		12.5	12.5		dB
Output Power @ 1 dB compression	f=0.5 to 2.5 GHz		18.2	12		dBm
Output IP3	f=0.5 to 2.5 GHz		29	24		dBm
Noise Figure	f=0.5 to 2.5 GHz		5.5	5.5		dB
Directivity (Isolation-Gain)	f=0.5 to 2.5 GHz		18-24	16-25		dB
DC Current			85	80	105	mA
Thermal Resistance, junction-to-case[1]			125			°C/W

Absolute Maximum Ratings

Parameter	Ratings
Operating Temperature	-40°C to 85°C
Storage Temperature	-55°C to 150°C
DC Voltage	+7V, -1.0V reverse
Power Dissipation	1000mW
Input Power	10dBm

Note: Permanent damage may occur if any of these limits are exceeded.
These ratings are not intended for continuous normal operation.
[1]Case is defined as ground leads.

Product Marking



(pin1)

Additional Detailed Technical Information

Additional information is available on our web site. To access this information enter the model number on our web site home page.

Performance data, graphs, s-parameter data set (.zip file)

Case Style: XX211-1

VNA-25+: Plastic molded, 8-lead SOIC, lead finish: Tin Plate

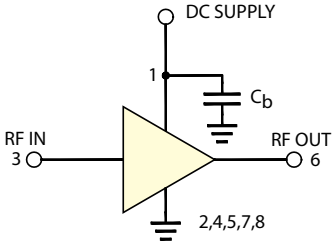
Tape & Reel: F16

Suggested Layout for PCB Design: PL-077

Evaluation Board: TB-01

Environmental Ratings: ENV08T1

Recommended Application Circuit



C_b= 100pF to 10 nF

Test Board includes case, connectors, and components (in bold) soldered to PCB

Sept. 1995
Edition 3.0a

FUJITSU

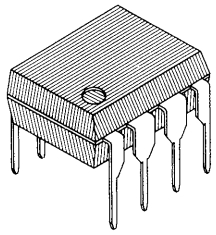
DATA SHEET

MB506

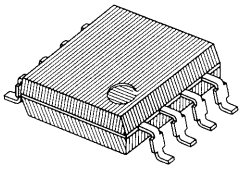
ULTRA HIGH FREQUENCY PRESCALER

ULTRA HIGH FREQUENCY PRESCALER

The Fujitsu MB506 is a high frequency, up to 2.4GHz, prescaler used with a frequency synthesizer to form a Phase Locked Loop (PLL). It will divide the input frequency by the modulus of 128 or 256 and the output level is 1.6V peak to peak on ECL level.Operation in the 1.6GHz range meets the specification for applications in Direct Broadcasting Satellite Systems (DBS), CATV systems, and UHF Transceivers.



PLASTIC PACKAGE
DIP-08P-M01

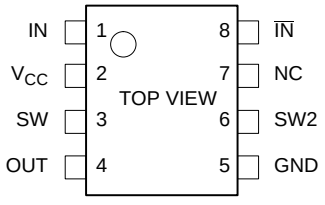


PLASTIC PACKAGE
FPT-08P-M01

FEATURES

- High Frequency Operation 2.4GHz max.
- Power Dissipation 90mW typ.
- Wide Operation Temperature -40°C to +85°C
- Stable Output Amplitude $V_{OUT} = 1.6V_{p-p}$
- Complete PLL synthesizer circuit with the Fujitsu MB87006A, PLL synthesizer IC
- Plastic 8-pin Standard Dual-In-Line Package or Flat Package

PIN ASSIGNMENT



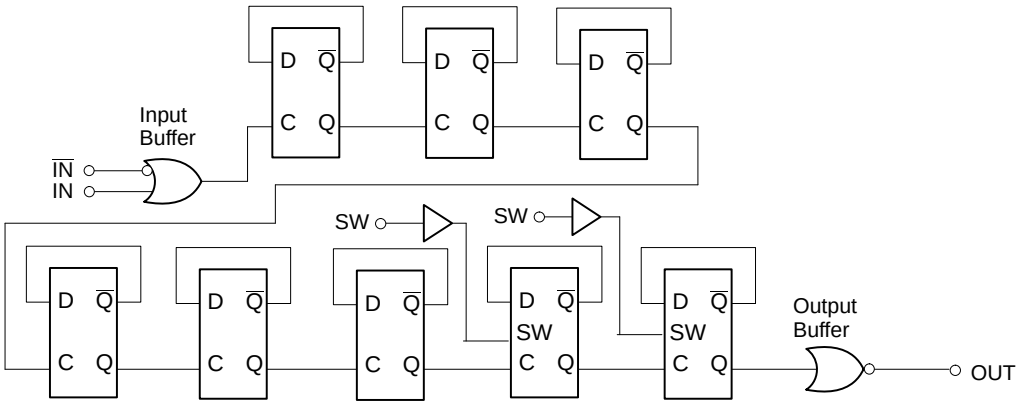
ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	–0.5 to +7.0	V
Input Voltage	V_{IN}	–0.5 to V_{CC}	V
Output Current	I_O	10	mA
Storage Temperature	T_{STG}	–55 to +125	°C

Note: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



SW1	SW2	Divide Ratio
H	H	1/64
L	H	1/128
H	L	1/128
L	L	1/256

Note: H = V_{CC}, L = open

Figure 1. MB506 Block Diagram

PIN DESCRIPTION

Pin Number	Symbol	Function
1	IN	Input
2	V_{CC}	Power Supply Voltage
3	SW1	Divide Ratio Control Input Selecting Divide Ratio (See Divide Ratio Table)
4	OUT	Output
5	GND	Ground
6	SW2	Divide Ratio Control Input Selecting Divide Ratio (See Divide Ratio Table)
7	NC	No Connection
8	$\overline{IN}$	Complementary Input

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Output Current	I_O		1.2		mA
Ambient Temperature	T_A	–40		+85	°C
Load Capacitance	C_L			12	pF

ELECTRICAL CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Conditions		Value			Unit
				Min.	Typ.	Max.	
Supply Curent	I_{CC}				18		mA
Output Amplitude	V_O			1.0	1.6		V_{p-p}
Input Frequency	f_{IN}	with input coupling capacitor 1000pF	T_A = –40°C to 85°C	100		2200	MHz
			T_A = –40°C to 60°C	100		2400	
Input Signal Amplitude	P_{IN}	f_{IN} = 100MHz to 1.3GHz		–16		5.5	dBm
		f_{IN} = 1.3MHz to 2.4GHz		–4		5.5	
High Level Input Voltage for SW	V_{IHS}*			V_{CC} –0.1	V_{CC}	V_{CC} +0.1	V
Low Level Input Voltage for SW	V_{ILS}			Open			V

Note: *Design Guarantee

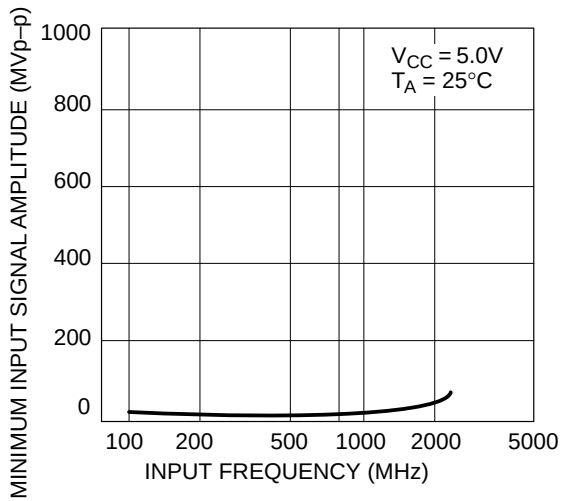
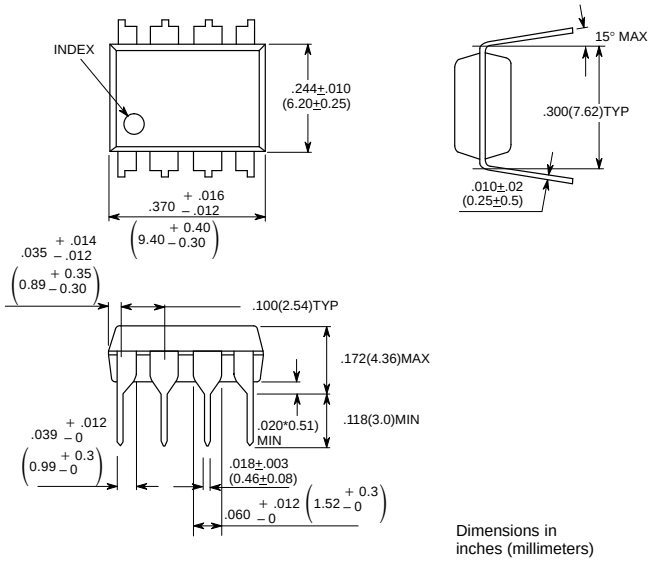


Figure 2. Input Signal Amplitude vs. Input Frequency

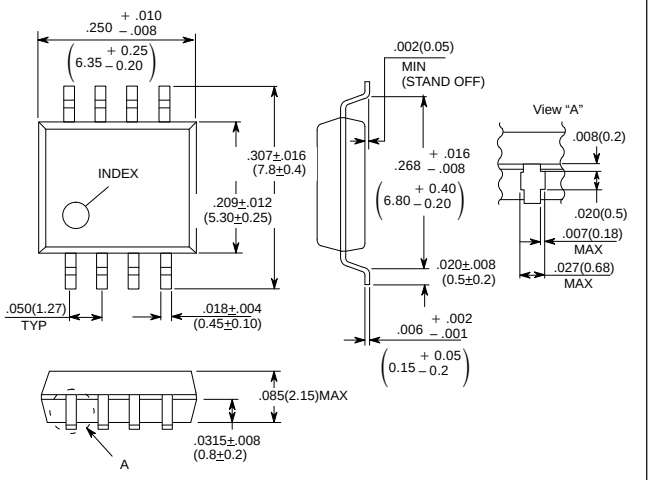
PACKAGE DIMENSIONS

8-LEAD PLASTIC DUAL-IN-LINE PACKAGE
(CASE No.: DIP-08P-M01)



Dimensions in
inches (millimeters)

8-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-08P-M01)



Dimensions in
inches (millimeters)

FUJITSU LIMITED

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Printed in Japan PV0050–902A3

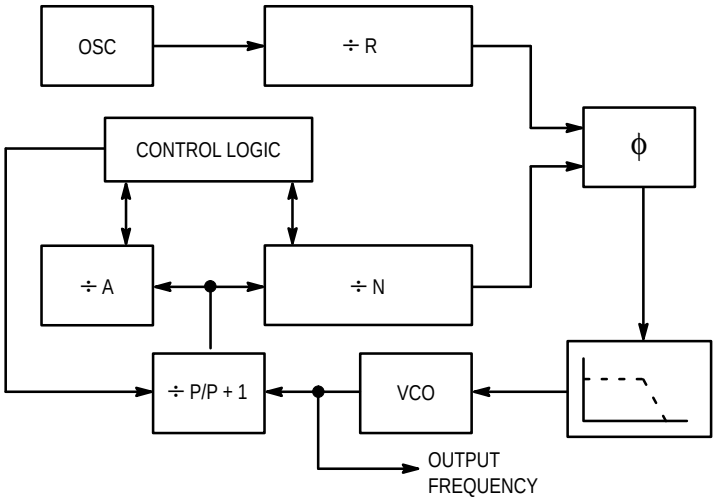
MC145151-2
MC145152-2
MC145155-2
MC145156-2
MC145157-2
MC145158-2

PLL Frequency Synthesizer Family
CMOS

The devices described in this document are typically used as low–power, phase–locked loop frequency synthesizers. When combined with an external low–pass filter and voltage–controlled oscillator, these devices can provide all the remaining functions for a PLL frequency synthesizer operating up to the device's frequency limit. For higher VCO frequency operation, a down mixer or a prescaler can be used between the VCO and the synthesizer IC.

These frequency synthesizer chips can be found in the following and other applications:

CATV	TV Tuning
AM/FM Radios	Scanning Receivers
Two–Way Radios	Amateur Radio



CONTENTS

REV 1
8/95

MC145151-2

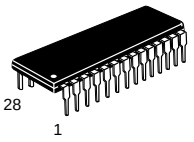
Parallel-Input PLL Frequency Synthesizer

Interfaces with Single–Modulus Prescalers

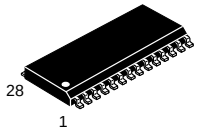
The MC145151–2 is programmed by 14 parallel–input data lines for the N counter and three input lines for the R counter. The device features consist of a reference oscillator, selectable–reference divider, digital–phase detector, and 14–bit programmable divide–by–N counter.

The MC145151–2 is an improved–performance drop–in replacement for the MC145151–1. The power consumption has decreased and ESD and latch–up performance have improved.

- Operating Temperature Range: – 40 to 85°C
- Low Power Consumption Through Use of CMOS Technology
- 3.0 to 9.0 V Supply Range
- On– or Off–Chip Reference Oscillator Operation
- Lock Detect Signal
- ÷ N Counter Output Available
- Single Modulus/Parallel Programming
- 8 User–Selectable ÷ R Values: 8, 128, 256, 512, 1024, 2048, 2410, 8192
- ÷ N Range = 3 to 16383
- “Linearized” Digital Phase Detector Enhances Transfer Function Linearity
- Two Error Signal Options: Single–Ended (Three–State) or Double–Ended
- Chip Complexity: 8000 FETs or 2000 Equivalent Gates



P SUFFIX
PLASTIC DIP
CASE 710

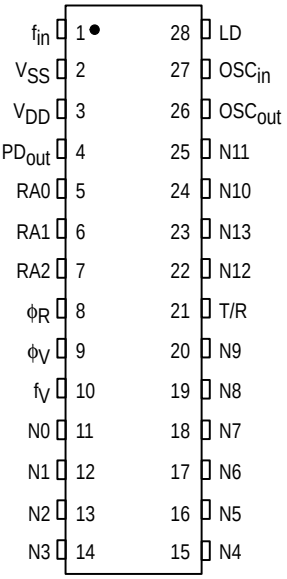


DW SUFFIX
SOG PACKAGE
CASE 751F

ORDERING INFORMATION

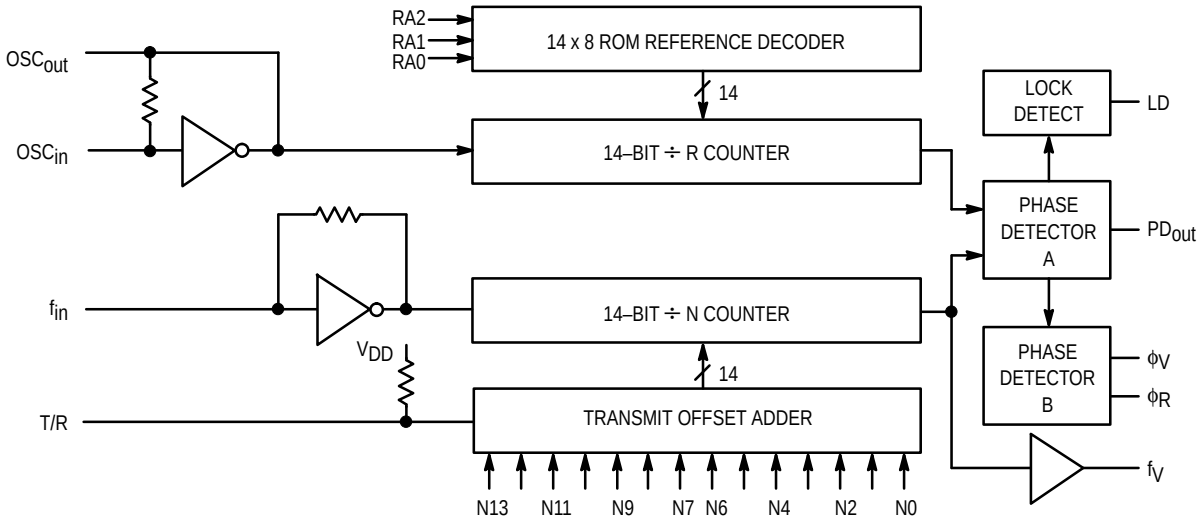
MC145151P2	Plastic DIP
MC145151DW2	SOG Package

PIN ASSIGNMENT



REV 1
8/95

MC145151–2 BLOCK DIAGRAM



NOTE: N0 – N13 inputs and inputs RA0, RA1, and RA2 have pull–up resistors that are not shown.

PIN DESCRIPTIONS

INPUT PINS

f_{in}
Frequency Input (Pin 1)

Input to the ÷ N portion of the synthesizer. f_{in} is typically derived from loop VCO and is ac coupled into the device. For larger amplitude signals (standard CMOS logic levels) dc coupling may be used.

RA0 – RA2
Reference Address Inputs (Pins 5, 6, 7)

These three inputs establish a code defining one of eight possible divide values for the total reference divider, as defined by the table below.

Pull–up resistors ensure that inputs left open remain at a logic 1 and require only a SPST switch to alter data to the zero state.

Reference Address Code			Total Divide Value
RA2	RA1	RA0	
0	0	0	8
0	0	1	128
0	1	0	256
0	1	1	512
1	0	0	1024
1	0	1	2048
1	1	0	2410
1	1	1	8192

N0 – N11
N Counter Programming Inputs (Pins 11 – 20, 22 – 25)

These inputs provide the data that is preset into the ÷ N counter when it reaches the count of zero. N0 is the least significant and N13 is the most significant. Pull–up resistors ensure that inputs left open remain at a logic 1 and require only an SPST switch to alter data to the zero state.

T/R
Transmit/Receive Offset Adder Input (Pin 21)

This input controls the offset added to the data provided at the N inputs. This is normally used for offsetting the VCO frequency by an amount equal to the IF frequency of the transceiver. This offset is fixed at 856 when T/R is low and gives no offset when T/R is high. A pull–up resistor ensures that no connection will appear as a logic 1 causing no offset addition.

OSC_{in}, OSC_{out}
Reference Oscillator Input/Output (Pins 27, 26)

These pins form an on–chip reference oscillator when connected to terminals of an external parallel resonant crystal. Frequency setting capacitors of appropriate value must be connected from OSC_{in} to ground and OSC_{out} to ground. OSC_{in} may also serve as the input for an externally–generated reference signal. This signal is typically ac coupled to OSC_{in}, but for larger amplitude signals (standard CMOS logic levels) dc coupling may also be used. In the external reference mode, no connection is required to OSC_{out}.

OUTPUT PINS

PD_{out}
Phase Detector A Output (Pin 4)

Three–state output of phase detector for use as loop–error signal. Double–ended outputs are also available for this purpose (see ϕ_V and ϕ_R).

Frequency $f_V > f_R$ or f_V Leading: Negative Pulses
Frequency $f_V < f_R$ or f_V Lagging: Positive Pulses
Frequency $f_V = f_R$ and Phase Coincidence: High–Impedance State

ϕR, ϕV
Phase Detector B Outputs (Pins 8, 9)

These phase detector outputs can be combined externally for a loop–error signal. A single–ended output is also available for this purpose (see **PD_{out}**).

If frequency f_V is greater than f_R or if the phase of f_V is leading, then error information is provided by ϕ_V pulsing low. ϕ_R remains essentially high.

If the frequency f_V is less than f_R or if the phase of f_V is lagging, then error information is provided by ϕ_R pulsing low. ϕ_V remains essentially high.

If the frequency of $f_V = f_R$ and both are in phase, then both ϕ_V and ϕ_R remain high except for a small minimum time period when both pulse low in phase.

f_V
N Counter Output (Pin 10)

This is the buffered output of the ÷ N counter that is internally connected to the phase detector input. With this output available, the ÷ N counter can be used independently.

LD
Lock Detector Output (Pin 28)

Essentially a high level when loop is locked (f_R, f_V of same phase and frequency). Pulses low when loop is out of lock.

POWER SUPPLY

V_{DD}
Positive Power Supply (Pin 3)

The positive power supply potential. This pin may range from + 3 to + 9 V with respect to V_{SS}.

V_{SS}
Negative Power Supply (Pin 2)

The most negative supply potential. This pin is usually ground.

TYPICAL APPLICATIONS

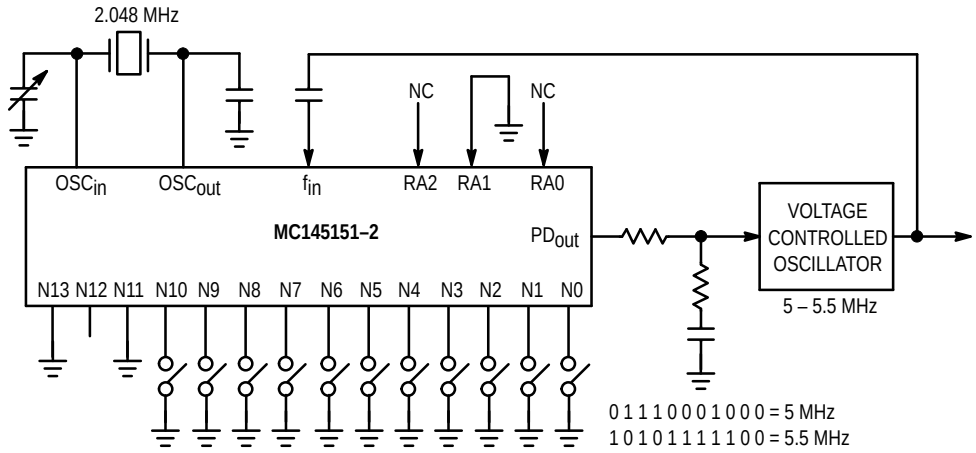
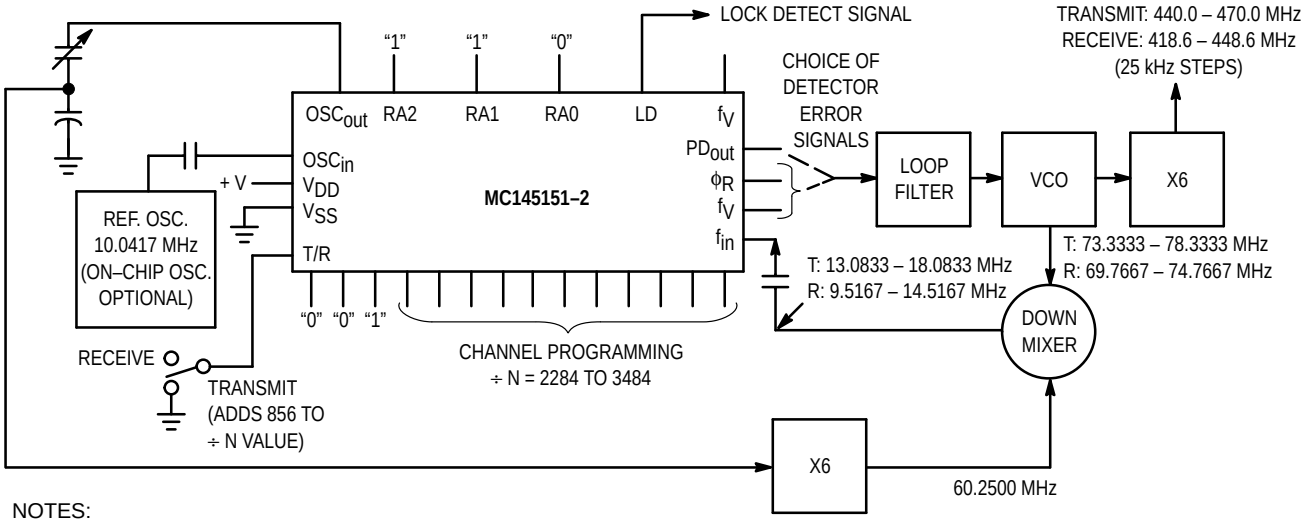


Figure 1. 5 MHz to 5.5 MHz Local Oscillator Channel Spacing = 1 kHz

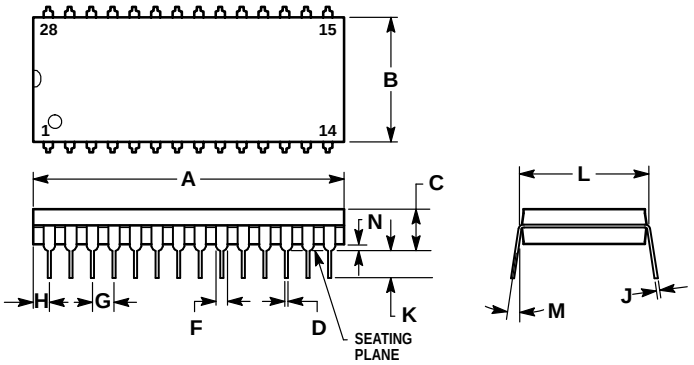


NOTES:
1. f_R = 4.1667 kHz; ÷ R = 2410; 21.4 MHz low side injection during receive.
2. Frequency values shown are for the 440 – 470 MHz band. Similar implementation applies to the 406 – 440 MHz band. For 470 – 512 MHz, consider reference oscillator frequency X9 for mixer injection signal (90.3750 MHz).

Figure 2. Synthesizer for Land Mobile Radio UHF Bands

MC145151–2 Data Sheet Continued on Page 23

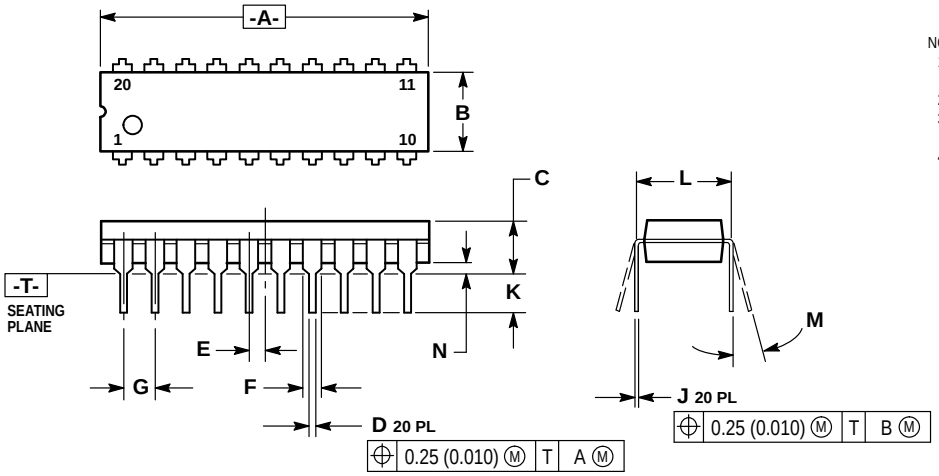
P SUFFIX
PLASTIC DIP
CASE 710–02
(MC145151–2, MC145152–2)



NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25mm (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	36.45	37.21	1.435	1.465
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

P SUFFIX
PLASTIC DIP
CASE 738–03
(MC145156–2)



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.010	1.070	25.66	27.17
B	0.240	0.260	6.10	6.60
C	0.150	0.180	3.81	4.57
D	0.015	0.022	0.39	0.55
E	0.050 BSC		1.27 BSC	
F	0.050	0.070	1.27	1.77
G	0.100 BSC		2.54 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.140	2.80	3.55
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

tyco Electronics

MACOM

Voltage Variable Absorptive Attenuator 30 dB, 0.5-2.0 GHz

AT-110 V4

Features

- Single Positive Voltage Control: 0 to +5 Volts
- 30 dB Voltage Variable Attenuation
- ± 2 dB Linearity from BSL
- Low DC Power Consumption
- Temperature Range: -40°C to +85°C
- SOIC-8 Plastic Package
- Tape and Reel Packaging Available
- Fast Switching Speed

Description

M/A-COM's AT-110 is a GaAs MMIC voltage variable absorptive attenuator in a low-cost SOIC 8-lead surface mount plastic package. The AT-110 has a faster switching speed than the AT-108 or AT-109. The AT-110 is ideally suited for use where linear attenuation fine tuning and very low power consumption are required.

Typical applications include radio, cellular, GPS equipment and automatic gain/level control circuits.

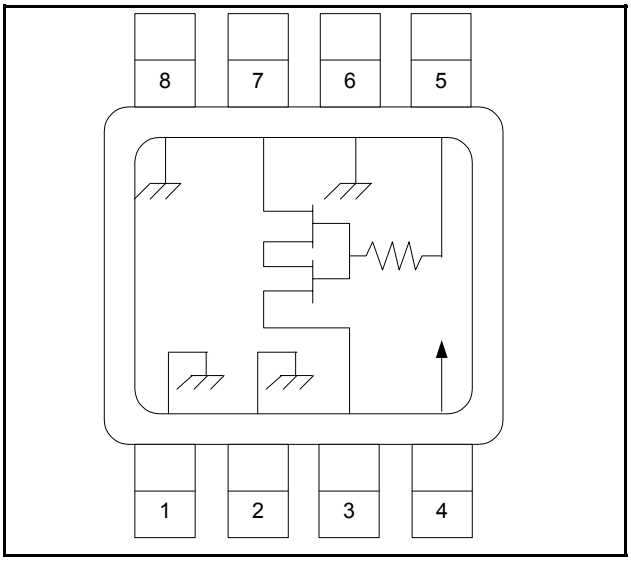
The AT-110 is fabricated with a monolithic GaAs MMIC using a mature 1-micron process. The process features full chip passivation for increased performance and reliability.

Ordering Information

Part Number	Package
AT-110	SOIC 8-Lead Plastic Package
AT-110TR	Forward Tape and Reel

Note: Reference Application Note M513 for reel size information.

Functional Schematic [1,2,3]



1. V_{CC} = +5 VDC ± 0.5 VDC @ 300 µA maximum.
2. V_C = 0 VDC to +5 VDC @ 6 mA maximum.
3. External DC blocking capacitors are required on all RF ports.

Pin Configuration

Pin No.	Function	Pin No.	Function
1	Ground	5	V_C
2	Ground	6	Ground
3	RF Port	7	RF Port
4	V_{CC}	8	Ground

Absolute Maximum Ratings [4]

Parameter	Absolute Maximum
Input Power	+21 dBm
Supply Voltage V_{CC}	-1 V ≤ V_{CC} ≤ +8 V
Control Voltage V_C	-1 V ≤ V_C ≤ V_{CC} + 0.5 V
Operating Temperature	-40°C to +85°C
Storage Temperature	-65°C to +150°C

4. Exceeding any one or combination of these limits may cause permanent damage to this device.

- **North America** Tel: 800.366.2266 / Fax: 978.366.2266
- **Europe** Tel: 44.1908.574.200 / Fax: 44.1908.574.300
- **Asia/Pacific** Tel: 81.44.844.8296 / Fax: 81.44.844.8298

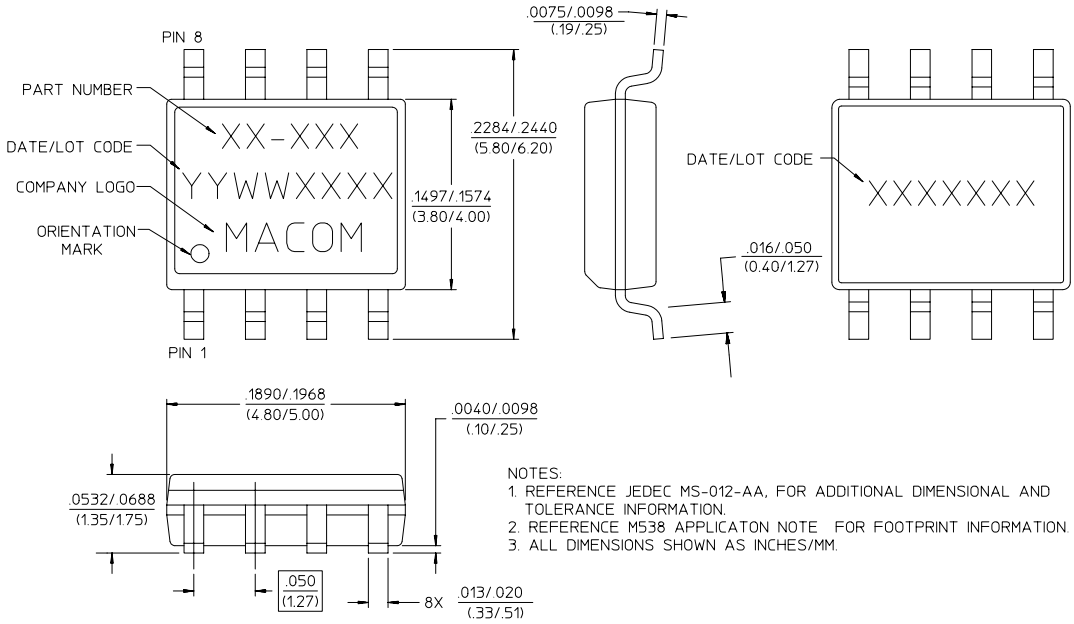
Visit www.macom.com for additional data sheets and product information.

Electrical Specifications[5]: T_A = 25°C, Z_0 = 50 Ω

Parameter	Test Conditions	Units	Min	Typ	Max
Insertion Loss	0.5 - 1.0 GHz 1.0 - 2.0 GHz	dB dB	— —	2.8 3.3	3.0 3.6
Attenuation	0.5 - 1.0 GHz 1.0 - 2.0 GHz	dB dB	30 25	— —	— —
Flatness (Peak to Peak)	0.5 - 1.0 GHz 1.0 - 2.0 GHz	dB dB	— —	± 0.5 ± 1.2	± 0.8 ± 1.5
VSWR	—	Ratio	—	2:1	—
Trise, Tfall	10% to 90% RF, 90% to 10% RF	µS	—	0.2	—
Ton, Toff	50% Control to 90% RF, 50% Control to 10% RF	µS	—	0.2	—
Transients	In-band	mV	—	70	—

5. The RF ports must be blocked outside of the package from ground or any other voltage.

SOIC-8



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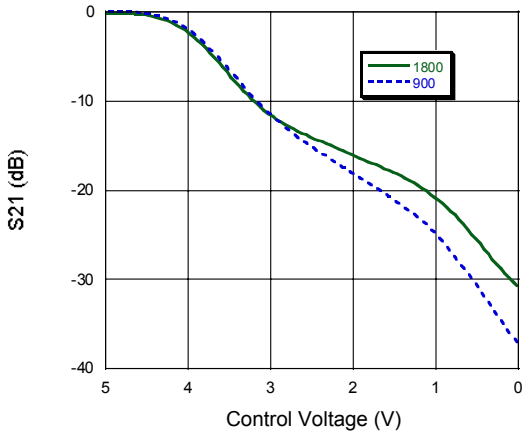
• **Asia/Pacific** Tel: 81.44.844.8296 / Fax: 81.44.844.8298

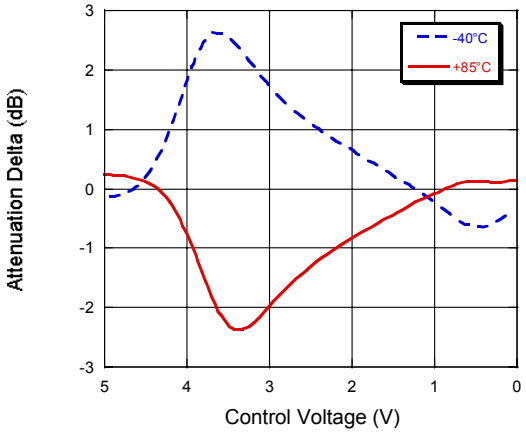
Visit www.macom.com for additional data sheets and product information.

Typical Performance Curves @ 25°C

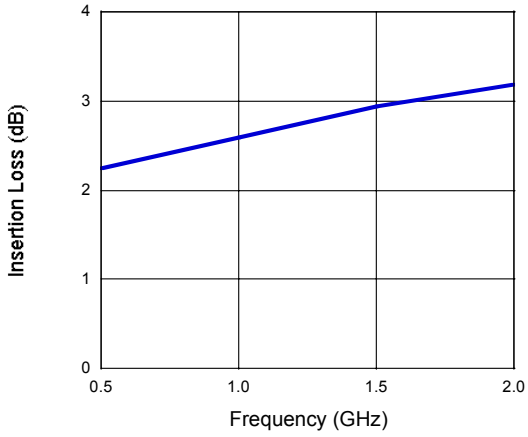
Attenuation vs. Control Voltage
F = 900, 1800 MHz



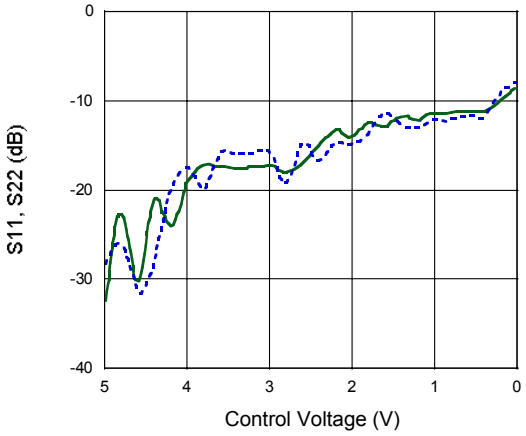
Attenuation vs. Temperature
Normalized to +25°C , F = 900 MHz



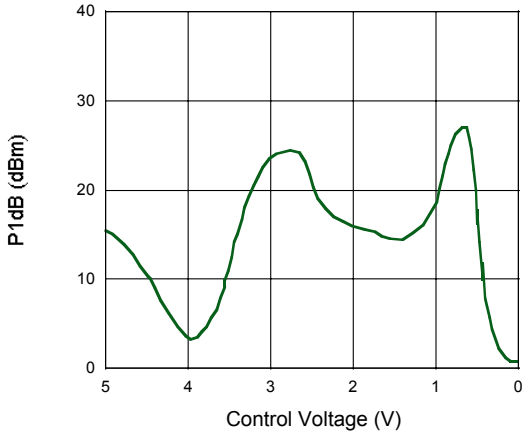
Insertion Loss vs. Frequency



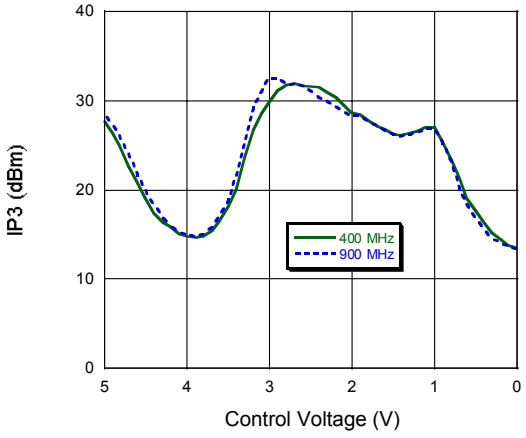
Return Loss vs. Control Voltage
F = 900 MHz



1 dB Compression vs. Control Voltage
F = 900 MHz



IP3 vs. Control Voltage



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• **Europe** Tel: 44.1908.574.200 / Fax: 44.1908.574.300
• **Asia/Pacific** Tel: 81.44.844.8296 / Fax: 81.44.844.8298

Visit www.macom.com for additional data sheets and product information.

19-1656; Rev 1; 2/02

MAXIM

High-Speed, Low-Voltage, 4Ω, Dual SPST CMOS Analog Switches

General Description

The MAX4641/MAX4642/MAX4643 are monolithic, dual, single-pole/single-throw (SPST) switches that can operate from a single supply ranging from +1.8V to +5.5V. The MAX4641/MAX4642/MAX4643 provide low 4Ω on-resistance (R_{ON}), 0.6Ω R_{ON} matching between channels, and 1Ω R_{ON} flatness over the entire analog signal range. These devices offer fast switching times of less than 20ns while consuming less than 0.01µW of quiescent power.

The MAX4641 has two normally open (NO) switches, and the MAX4642 has two normally closed (NC) switches. The MAX4643 has one NO switch and one NC switch. All three devices have low 0.35nA leakage currents over the entire temperature range. The MAX4641/MAX4642/MAX4643 are available in small 8-pin µMAX and 8-pin QFN packages.

Applications

Battery-Operated Equipment

Audio and Video Signal Routing

Low-Voltage Data-Acquisition Systems

Sample-and-Hold Circuits

Communications Circuits

Rail-to-Rail is a trademark of Nippon Motorola, Ltd.

Features

- **+1.8V to +5.5V Single-Supply Operation**
- **Rail-to-Rail™ Analog Signal Range**
- **Guaranteed R_{ON}**
  - **4Ω max (+5V supply)**
  - **8Ω max (+3V supply)**
- **+1.8V Operation**
  - **R_{ON} 30Ω typ Over Temperature**
  - **t_{ON} 18ns typ, t_{OFF} 12ns typ**
- **Guaranteed R_{ON} Flatness: 1Ω (+5V supply)**
- **Guaranteed R_{ON} Match Between Channels**
  - **0.6Ω (+5V supply)**
- **Low Leakage (<0.35nA) Over Entire Temperature Range**
- **Excellent AC Characteristics**
  - **Low Crosstalk: -97dB at 1MHz**
  - **High Off-Isolation: -80dB at 1MHz**
  - **0.018% Total Harmonic Distortion**
- **Low Power Consumption: < 0.01µW**

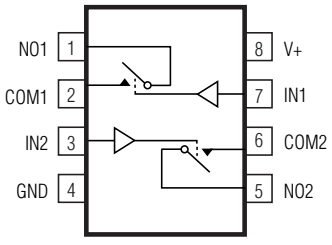
Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX4641EUA	-40°C to +85°C	8 µMAX
MAX4641EGA	-40°C to +85°C	8 QFN 3 x 3
MAX4642EUA	-40°C to +85°C	8 µMAX
MAX4642EGA	-40°C to +85°C	8 QFN 3 x 3
MAX4643EUA	-40°C to +85°C	8 µMAX
MAX4643EGA	-40°C to +85°C	8 QFN 3 x 3

Pin Configurations/Functional Diagrams/Truth Tables

TOP VIEW

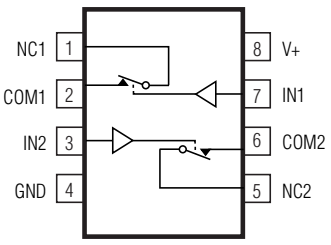
MAXIM *MAX4641*



µMAX

MAX4641	
IN_	**NO_**
0	OFF
1	ON

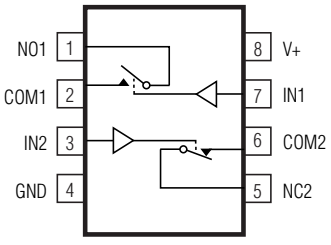
MAXIM *MAX4642*



µMAX

MAX4642	
IN_	**NC_**
0	ON
1	OFF

MAXIM *MAX4643*



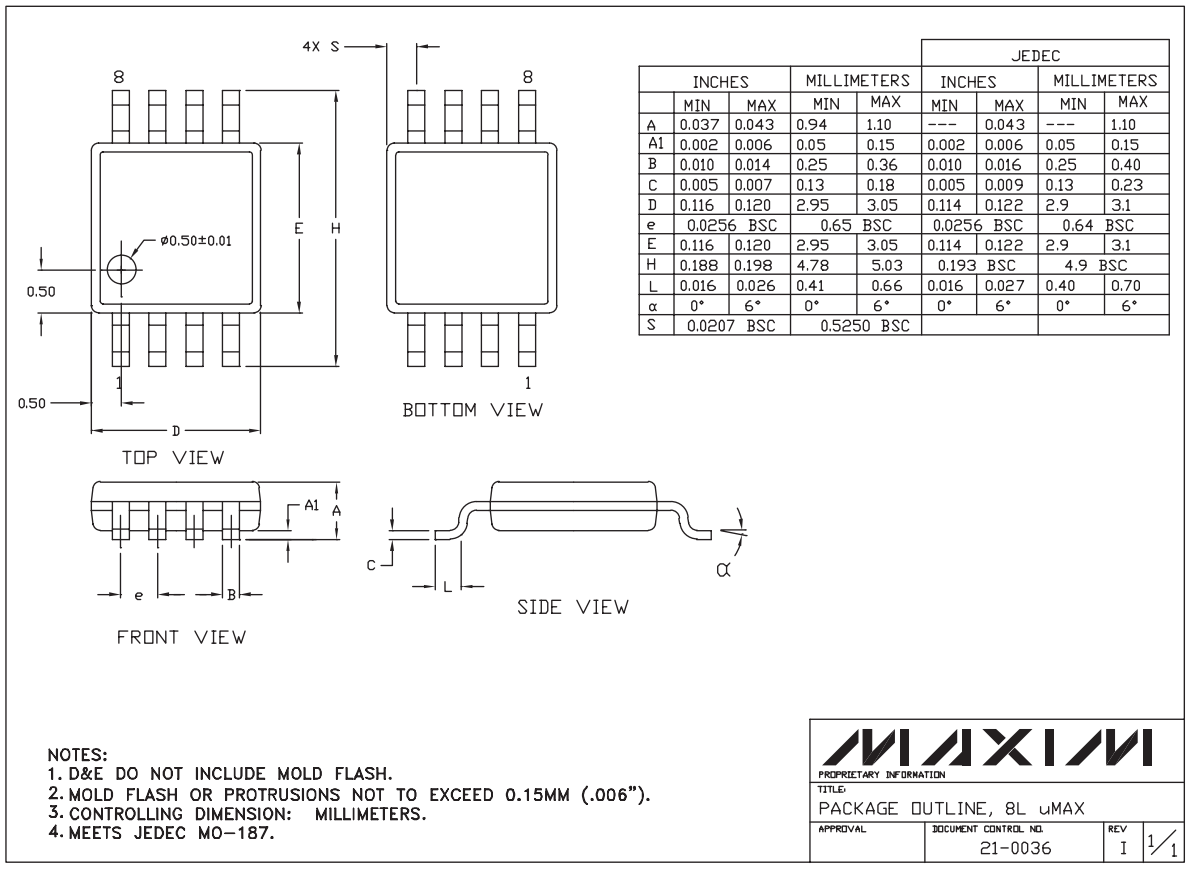
µMAX

MAX4643		
IN_	**NO1**	**NC2**
0	OFF	ON
1	ON	OFF

Pin Configurations continued at end of data sheet.

High-Speed, Low-Voltage, 4Ω, Dual SPST CMOS Analog Switches

Package Information



	INCHES		MILLIMETERS		JEDEC INCHES		JEDEC MILLIMETERS	
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	0.037	0.043	0.94	1.10	---	0.043	---	1.10
A1	0.002	0.006	0.05	0.15	0.002	0.006	0.05	0.15
B	0.010	0.014	0.25	0.36	0.010	0.016	0.25	0.40
C	0.005	0.007	0.13	0.18	0.005	0.009	0.13	0.23
D	0.116	0.120	2.95	3.05	0.114	0.122	2.9	3.1
e	0.0256 BSC		0.65 BSC		0.0256 BSC		0.64 BSC	
E	0.116	0.120	2.95	3.05	0.114	0.122	2.9	3.1
H	0.188	0.198	4.78	5.03	0.193 BSC		4.9 BSC	
L	0.016	0.026	0.41	0.66	0.016	0.027	0.40	0.70
α	0°	6°	0°	6°	0°	6°	0°	6°
S	0.0207 BSC		0.5250 BSC					

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15MM (.006").
3. CONTROLLING DIMENSION: MILLIMETERS.
4. MEETS JEDEC MO-187.

MAXIM
PROPRIETARY INFORMATION
TITLE: PACKAGE OUTLINE, 8L uMAX
APPROVAL | DOCUMENT CONTROL NO. 21-0036 | REV I | 1/1

LM2904,LM358/LM358A,LM258/LM258A

Dual Operational Amplifier

Features

- Internally Frequency Compensated for Unity Gain
- Large DC Voltage Gain: 100dB
- Wide Power Supply Range:
  LM258/LM258A, LM358/LM358A: 3V~32V (or ±1.5V ~ 16V)
  LM2904 : 3V~26V (or ±1.5V ~ 13V)
- Input Common Mode Voltage Range Includes Ground
- Large Output Voltage Swing: 0V DC to Vcc -1.5V DC
- Power Drain Suitable for Battery Operation.

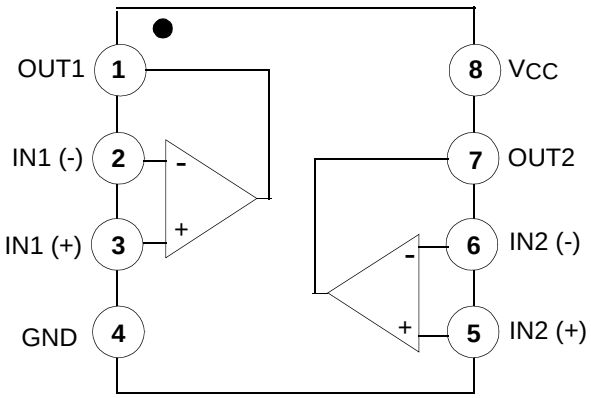
Description

The LM2904,LM358/LM358A, LM258/LM258A consist of two independent, high gain, internally frequency compensated operational amplifiers which were designed specifically to operate from a single power supply over a wide range of voltage. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage. Application areas include transducer amplifier, DC gain blocks and all the conventional OP-AMP circuits which now can be easily implemented in single power supply systems.

8-DIP

8-SOP

Internal Block Diagram

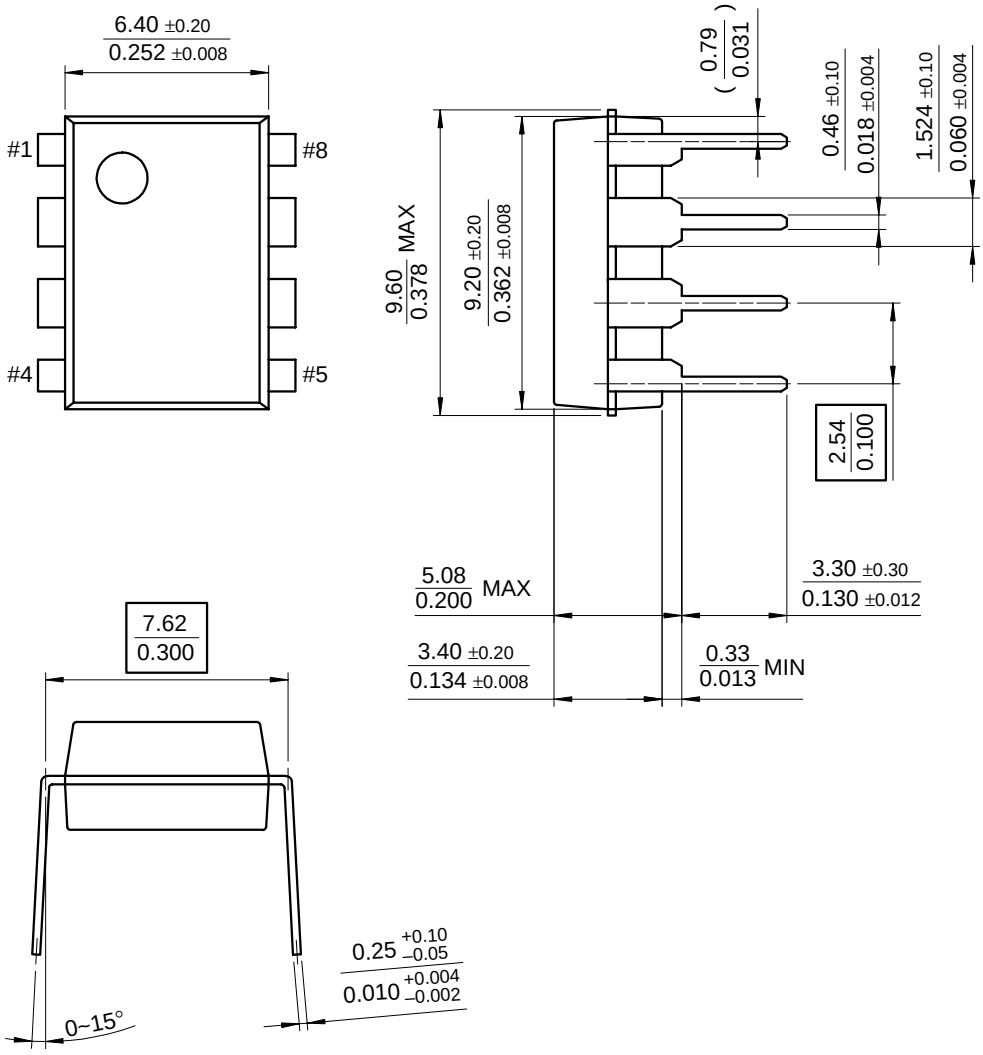


Mechanical Dimensions

Package

Dimensions in millimeters

8-DIP



- **Low Power Consumption**
- **Wide Common-Mode and Differential Voltage Ranges**
- **Low Input Bias and Offset Currents**
- **Output Short-Circuit Protection**
- **Low Total Harmonic Distortion . . . 0.003% Typ**
- **High Input Impedance . . . JFET-Input Stage**
- **Latch-Up-Free Operation**
- **High Slew Rate . . . 13 V/μs Typ**
- **Common-Mode Input Voltage Range Includes V_{CC+}**

description/ordering information

The TL08x JFET-input operational amplifier family is designed to offer a wider selection than any previously developed operational amplifier family. Each of these JFET-input operational amplifiers incorporates well-matched, high-voltage JFET and bipolar transistors in a monolithic integrated circuit. The devices feature high slew rates, low input bias and offset currents, and low offset-voltage temperature coefficient. Offset adjustment and external compensation options are available within the TL08x family.

The C-suffix devices are characterized for operation from 0°C to 70°C. The I-suffix devices are characterized for operation from −40°C to 85°C. The Q-suffix devices are characterized for operation from −40°C to 125°C. The M-suffix devices are characterized for operation over the full military temperature range of −55°C to 125°C.

ORDERING INFORMATION

T_J	V_{IO}max AT 25°C	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	15 mV	PDIP (P)	Tube of 50	TL081CP	TL081CP
			Tube of 50	TL082CP	TL082CP
		PDIP (N)	Tube of 25	TL084CN	TL084CN
		SOIC (D)	Tube of 75	TL081CD	TL081C
			Reel of 2500	TL081CDR	
			Tube of 75	TL082CD	TL082C
			Reel of 2500	TL082CDR	
			Tube of 50	TL084CD	TL084C
			Reel of 2500	TL084CDR	
		SOP (PS)	Reel of 2000	TL081CPSR	T081
			Reel of 2000	TL082CPSR	T082
		SOP (NS)	Reel of 2000	TL084CNSR	TL084
		TSSOP (PW)	Tube of 150	TL082CPW	T082
			Reel of 2000	TL082CPWR	
			Tube of 90	TL084CPW	T084
			Reel of 2000	TL084CPWR	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

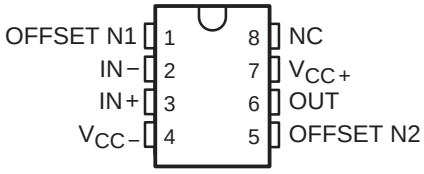
description/ordering information (continued)

ORDERING INFORMATION

T_J	V_{IO}max AT 25°C	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	6 mV	PDIP (P)	Tube of 50	TL081ACP	TL081ACP
			Tube of 50	TL082ACP	TL082ACP
		PDIP (N)	Tube of 25	TL084ACN	TL084ACN
		SOIC (D)	Tube of 75	TL081ACD	081AC
			Reel of 2500	TL081ACDR	
			Tube of 75	TL082ACD	082AC
			Reel of 2500	TL082ACDR	
			Tube of 50	TL084ACD	TL084AC
			Reel of 2500	TL084ACDR	
		SOP (PS)	Reel of 2000	TL082ACPSR	T082A
		SOP (NS)	Reel of 2000	TL084ACNSR	TL084A
	3 mV	PDIP (P)	Tube of 50	TL081BCP	TL081BCP
			Tube of 50	TL082BCP	TL082BCP
		PDIP (N)	Tube of 25	TL084BCN	TL084BCN
		SOIC (D)	Tube of 75	TL081BCD	081BC
			Reel of 2500	TL081BCDR	
			Tube of 75	TL082BCD	082BC
			Reel of 2500	TL082BCDR	
			Tube of 50	TL084BCD	TL084BC
			Reel of 2500	TL084BCDR	
−40°C to 85°C	6 mV	PDIP (P)	Tube of 50	TL081IP	TL081IP
			Tube of 50	TL082IP	TL082IP
		PDIP (N)	Tube of 25	TL084IN	TL081IN
		SOIC (D)	Tube of 75	TL081ID	TL081I
			Reel of 2500	TL081IDR	
			Tube of 75	TL082ID	TL082I
			Reel of 2500	TL082IDR	
			Tube of 50	TL084ID	TL084I
			Reel of 2500	TL084IDR	
		TSSOP (PW)	Reel of 2000	TL082IPWR	Z082
−40°C to 125°C	9 mV	SOIC (D)	Tube of 50	TL084QD	TL084QD
			Reel of 2500	TL084QDR	
−55°C to 125°C	9 mV	CDIP (J)	Tube of 25	TL084MJ	TL084MJ
		LCCC (FK)	Reel of 55	TL084FK	TL084FK
	6 mV	CDIP (JG)	Tube of 50	TL082MJG	TL082MJG
		LCCC (FK)	Tube of 55	TL082MFK	TL082MFK

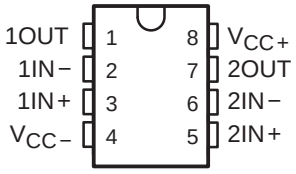
† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

TL081, TL081A, TL081B
D, P, OR PS PACKAGE
(TOP VIEW)

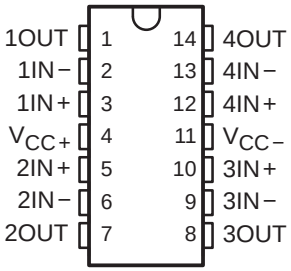


NC − No internal connection

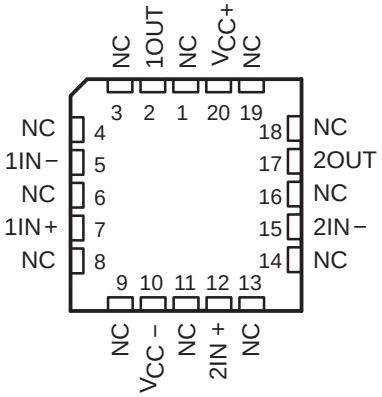
TL082, TL082A, TL082B
D, JG, P, PS, OR PW PACKAGE
(TOP VIEW)



TL084, TL084A, TL084B
D, J, N, NS, OR PW PACKAGE
(TOP VIEW)

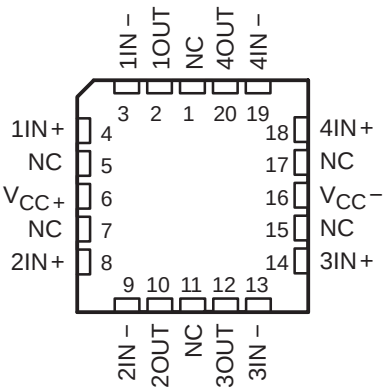


TL082M . . . FK PACKAGE
(TOP VIEW)



NC − No internal connection

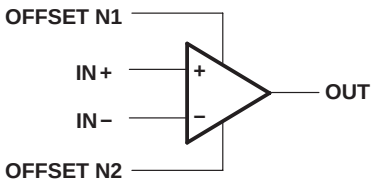
TL084M . . . FK PACKAGE
(TOP VIEW)



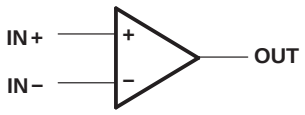
NC − No internal connection

symbols

TL081

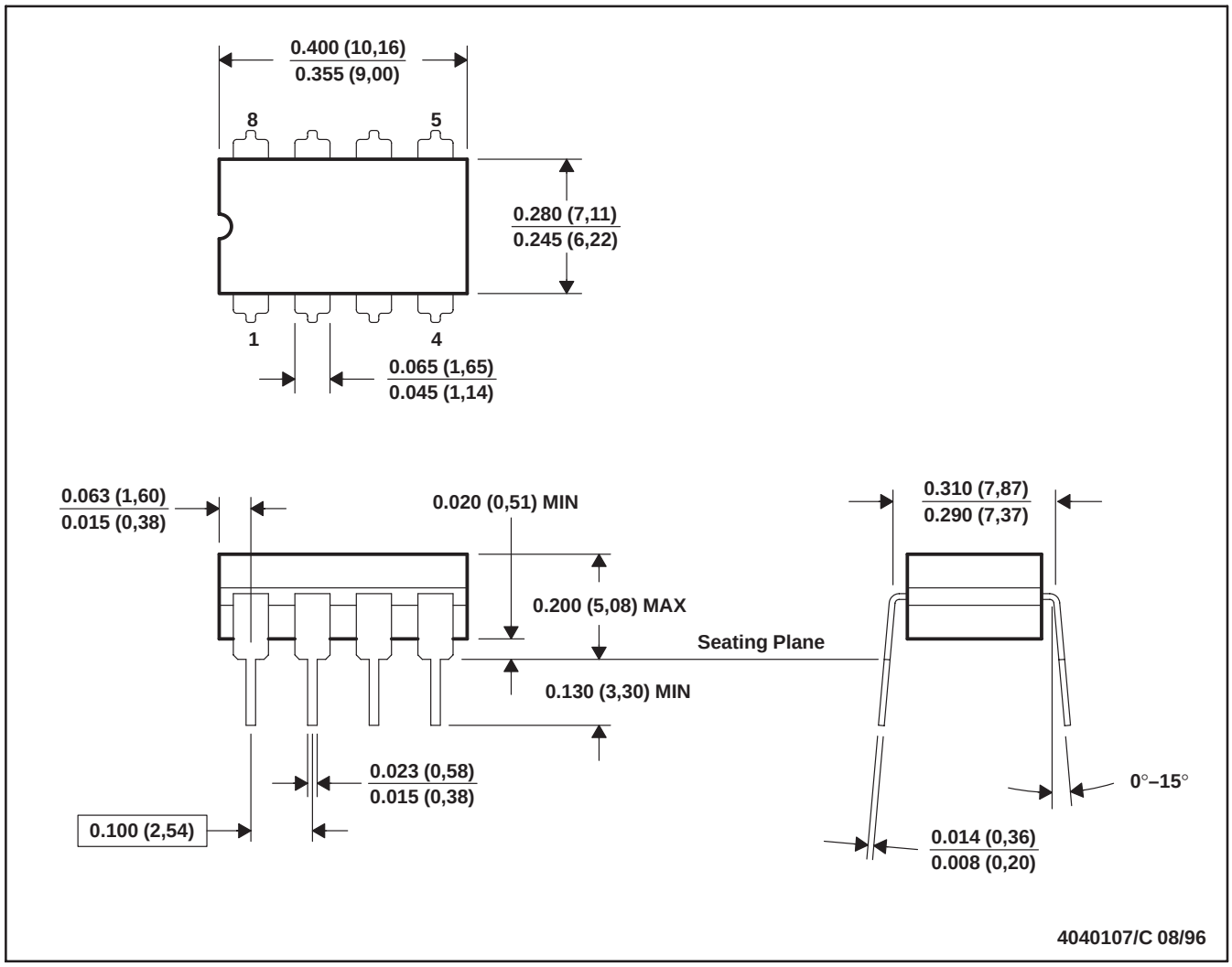


TL082 (EACH AMPLIFIER)
TL084 (EACH AMPLIFIER)



MCER001A – JANUARY 1995 – REVISED JANUARY 1997

JG (R-GDIP-T8) **CERAMIC DUAL-IN-LINE**



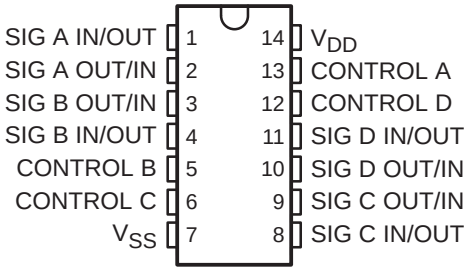
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification.
E. Falls within MIL STD 1835 GDIP1-T8

CD4066B
CMOS QUAD BILATERAL SWITCH

SCHS051D – NOVEMBER 1998 – REVISED SEPTEMBER 2003

- **15-V Digital or ±7.5-V Peak-to-Peak Switching**
- **125-Ω Typical On-State Resistance for 15-V Operation**
- **Switch On-State Resistance Matched to Within 5 Ω Over 15-V Signal-Input Range**
- **On-State Resistance Flat Over Full Peak-to-Peak Signal Range**
- **High On/Off Output-Voltage Ratio: 80 dB Typical at f_{is} = 10 kHz, R_L = 1 kΩ**
- **High Degree of Linearity: <0.5% Distortion Typical at f_{is} = 1 kHz, V_{is} = 5 V p-p, $V_{DD} - V_{SS} \geq$ 10 V, R_L = 10 kΩ**
- **Extremely Low Off-State Switch Leakage, Resulting in Very Low Offset Current and High Effective Off-State Resistance: 10 pA Typical at $V_{DD} - V_{SS}$ = 10 V, T_A = 25°C**
- **Extremely High Control Input Impedance (Control Circuit Isolated From Signal Circuit): 10^{12} Ω Typical**
- **Low Crosstalk Between Switches: –50 dB Typical at f_{is} = 8 MHz, R_L = 1 kΩ**
- **Matched Control-Input to Signal-Output Capacitance: Reduces Output Signal Transients**
- **Frequency Response, Switch On = 40 MHz Typical**
- **100% Tested for Quiescent Current at 20 V**
- **5-V, 10-V, and 15-V Parametric Ratings**
- **Meets All Requirements of JEDEC Tentative Standard No. 13-B, *Standard Specifications for Description of "B" Series CMOS Devices***
- **Applications:**
  - **Analog Signal Switching/Multiplexing: Signal Gating, Modulator, Squelch Control, Demodulator, Chopper, Commutating Switch**
  - **Digital Signal Switching/Multiplexing**
  - **Transmission-Gate Logic Implementation**
  - **Analog-to-Digital and Digital-to-Analog Conversion**
  - **Digital Control of Frequency, Impedance, Phase, and Analog-Signal Gain**

E, F, M, NS, OR PW PACKAGE
(TOP VIEW)



description/ordering information

The CD4066B is a quad bilateral switch intended for the transmission or multiplexing of analog or digital signals. It is pin-for-pin compatible with the CD4016B, but exhibits a much lower on-state resistance. In addition, the on-state resistance is relatively constant over the full signal-input range.

The CD4066B consists of four bilateral switches, each with independent controls. Both the p and the n devices in a given switch are biased on or off simultaneously by the control signal. As shown in Figure 1, the well of the n-channel device on each switch is tied to either the input (when the switch is on) or to V_{SS} (when the switch is off). This configuration eliminates the variation of the switch-transistor threshold voltage with input signal and, thus, keeps the on-state resistance low over the full operating-signal range.

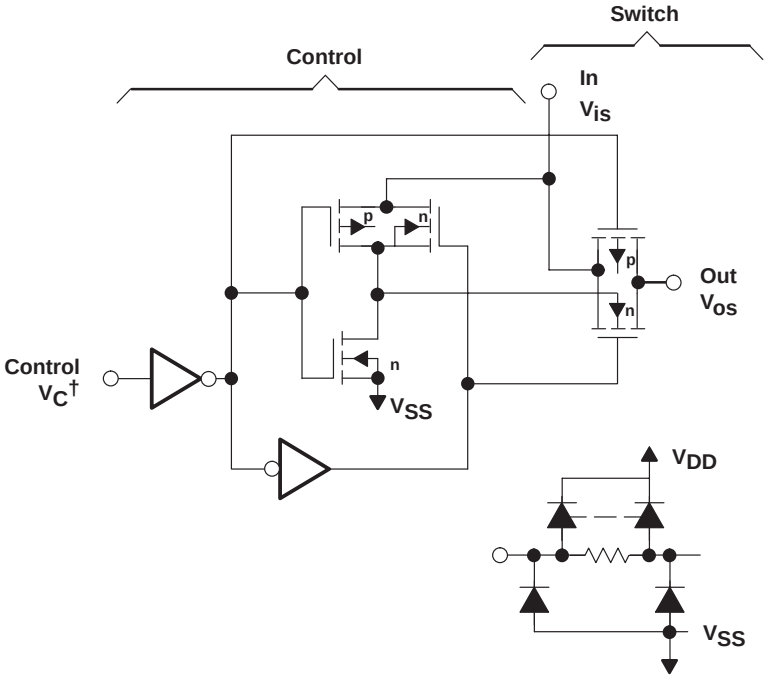
The advantages over single-channel switches include peak input-signal voltage swings equal to the full supply voltage and more constant on-state impedance over the input-signal range. However, for sample-and-hold applications, the CD4016B is recommended.

description/ordering information (continued)

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–55°C to 125°C	CDIP – F	Tube of 25	CD4066BF3A	CD4066BF3A
	PDIP – E	Tube of 25	CD4066BE	CD4066BE
	SOIC – M	Tube of 50	CD4066BM	CD4066BM
		Reel of 2500	CD4066BM96	
		Reel of 250	CD4066BMT	
	SOP – NS	Reel of 2000	CD4066BNSR	CD4066B
	TSSOP – PW	Tube of 90	CD4066BPW	CM066B
		Reel of 2000	CD4066BPWR	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



† All control inputs are protected by the CMOS protection network.

NOTES: A. All p substrates are connected to V_{DD}.
B. Normal operation control-line biasing: switch on (logic 1), $V_C = V_{DD}$; switch off (logic 0), $V_C = V_{SS}$
C. Signal-level range: $V_{SS} \le V_{is} \le V_{DD}$

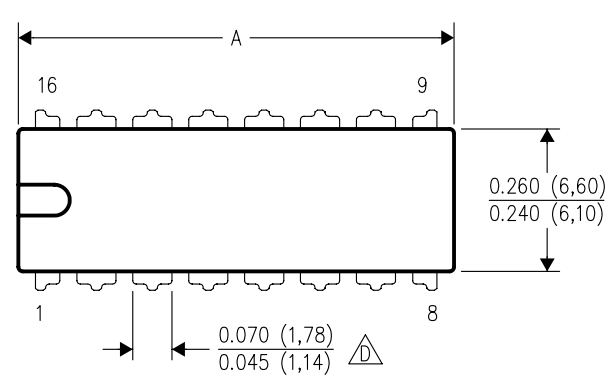
92CS-29113

Figure 1. Schematic Diagram of One-of-Four Identical Switches and Associated Control Circuitry

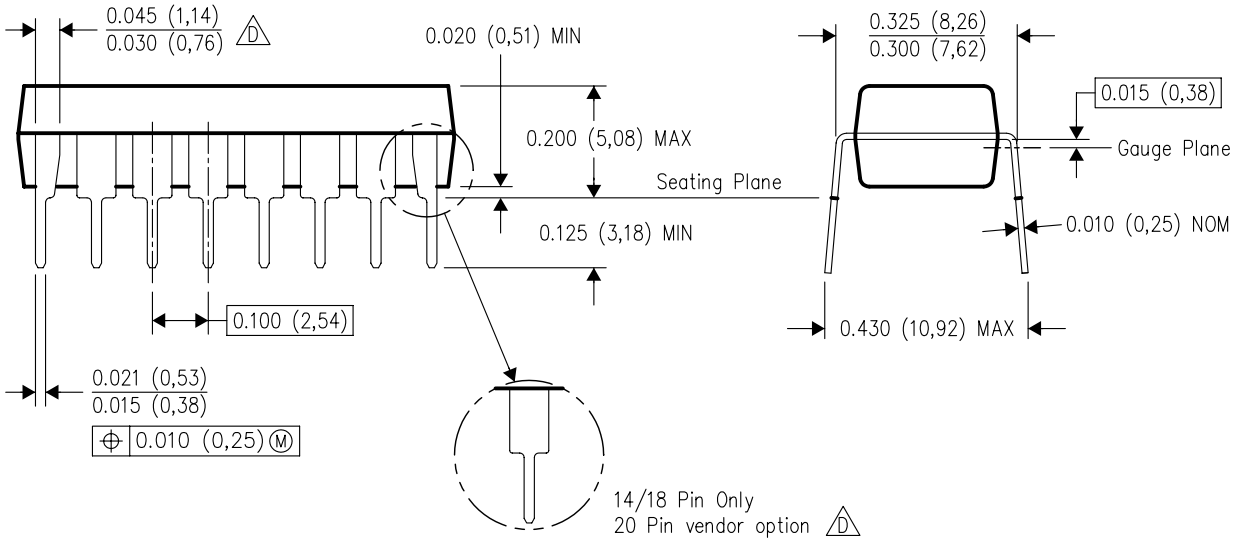
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.